OPERATING MANUAL

File: T 37

TELEGRAPH AND DATA SIGNAL ANALYSER

OPERATING INSTRUCTIONS

QUALITY ASSURANCE
STANDARDS, CALIBRATION, AND MAINTENANCE LAB.

TELEGRAPH AND DATA SIGNAL ANALYSER NO. 1A AND NO. 2A

OPERATING INSTRUCTIONS

1. Mains Supply Connection

Ensure that the mains voltage selector mounted on the rear panel is set correctly to accommodate the local supply voltage.

2. Start-Stop Distortion Measurement

2.1 Input Connection

Set the START/MARK element polarity switch to the appropriate position to conform with the incoming data, either positive (+) start and negative (-) mark, or negative start (-) and positive mark(+).

Set the Input Selector switch to the position giving the incoming data signalling method, either Double Current (D. CUR.) high level signalling or Single Current (S. CUR.) high level signalling of positive (+ve) or negative (-ve) polarity or low level +6v signalling with a V24 interface (V24).

2.1.1 Shunt Measurement

For high level telegraph signals connect the input wires between the input terminal referenced to the double and single current input switch positions and the Telegraph Earth terminal (TEL. EARTH).

Set the screwdriver slot switch mounted on the rear panel to SHUNT.

Set the input termination switch to low impedance (1K ohm) or high impedance (100K ohm) as required.

For the V24 signals connect the input wires between the input terminal referenced to the V24 input switch condition and the Common terminal (COMM).

For shunt measurements the Telegraph Earth/Common terminal may be connected to Protective Earth if required.

2.1.2 Series Measurement

Before operating the SERIES/SHUNT switch from SHUNT to SERIES ensure that the COMMON terminal is NOT connected to Protective Earth, and also that no other input is connected to the unit terminals.

The series measurement facility is intended for use with current signalling systems in the range 5 to 100mA, and at no time can the Telegraph Earth/Common terminal be connected to protective earth.

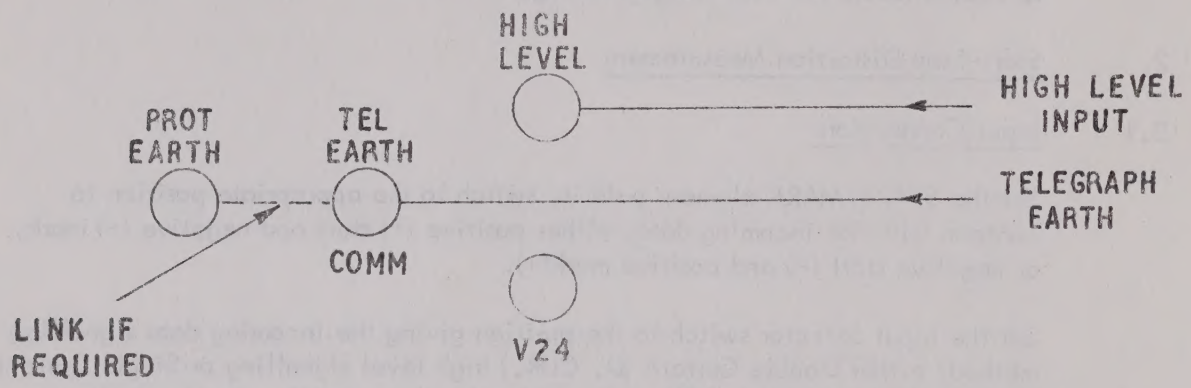
2.1.2 continued

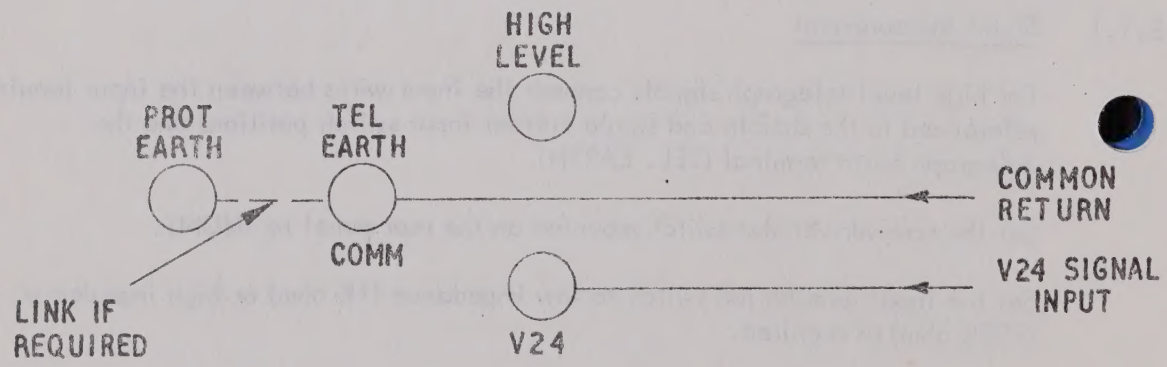
Set the screwdriver slot switch mounted on the rear panel to SERIES.

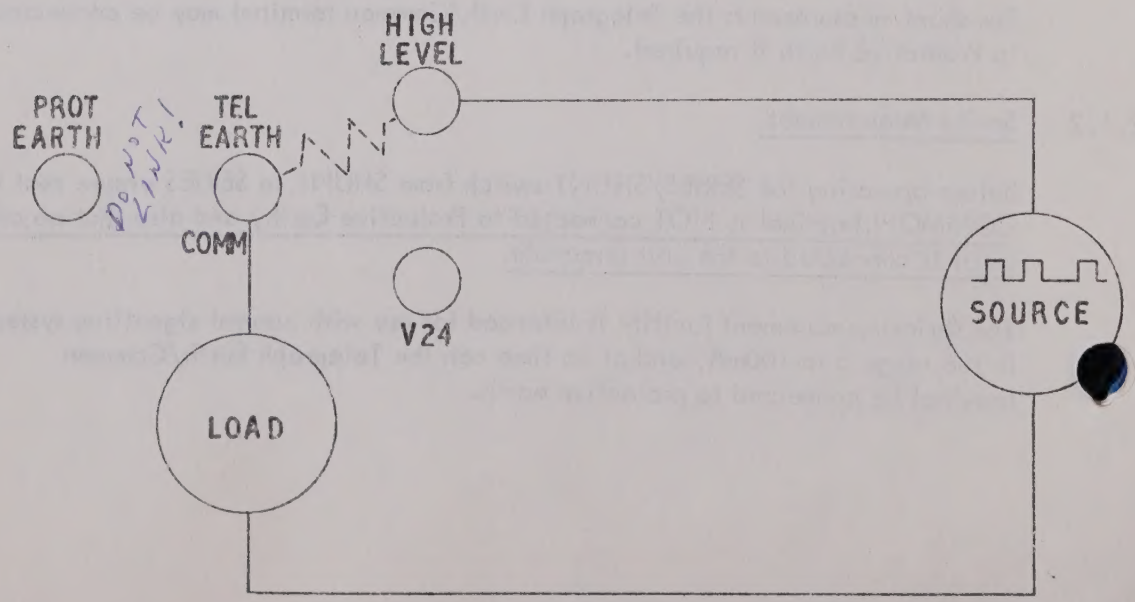
Connect the unit input in series with the line system through the high level input terminal and out of the Telegraph Earth/Common terminal.

Examples of the Shunt and Series connections are shown below:

Fig. 1 - High level shunt connection







2.2 Speed Setting

2.2.1 For standard data speeds set the oscillator selection switch to Calibrated (CAL).

Set the rotary speed switch to the appropriate speed, check that the toggle switch LOWER RANGE - UPPER RANGE is set correctly.

2.2.2 For non-standard data speeds set the rotary and range switches to give the nearest crystal speed.

Set the oscillator selection switch to Uncalibrated (UNCAL) and set the percentage potentiometer to give the required speed by adjusting the selected switched speed by up to ±20% as needed.

2.3 Measurement Mode

Set the measurement mode selection switch to START/STOP.

2.4 Display Control

2.4.1 Set the ELEMENTS PER CHARACTER switch to the number of information elements in the character code format being received.

2.4.2 Set the rotary display control switch to Hold Peak Distortion (HOLD PEAK DIST'N).

The display will now be triggered by each start element of the characters received and the transitions will be shown as upward deflections for positive transitions and downward deflections for negative transitions.

The transitions will be displayed in discrete 1% steps with bright up markers at 10% intervals to ease measurement readings.

The peak early and late distortions will be displayed and updated whilst information is being received. To reset the peak reading operate the push-button switch (RESET).

Each data transition within the characters will be superimposed to give all transitions on a single trace and they will be related to an ideal transition time at the centre of the trace.

2.4.3 Set the rotary display control switch to Separate Element Distortion (SEPARATE ELEMENT DIST'N). The display will be triggered by the start elements as in section 2.4.2.

Each data transition within the character will be allocated its own trace commencing with the transition at the end of the start element and finishing with the transition at the beginning of the stop element, with each trace covering the period 50% early to 50% late as shown below:

Fig. 4 - Separate Element Display

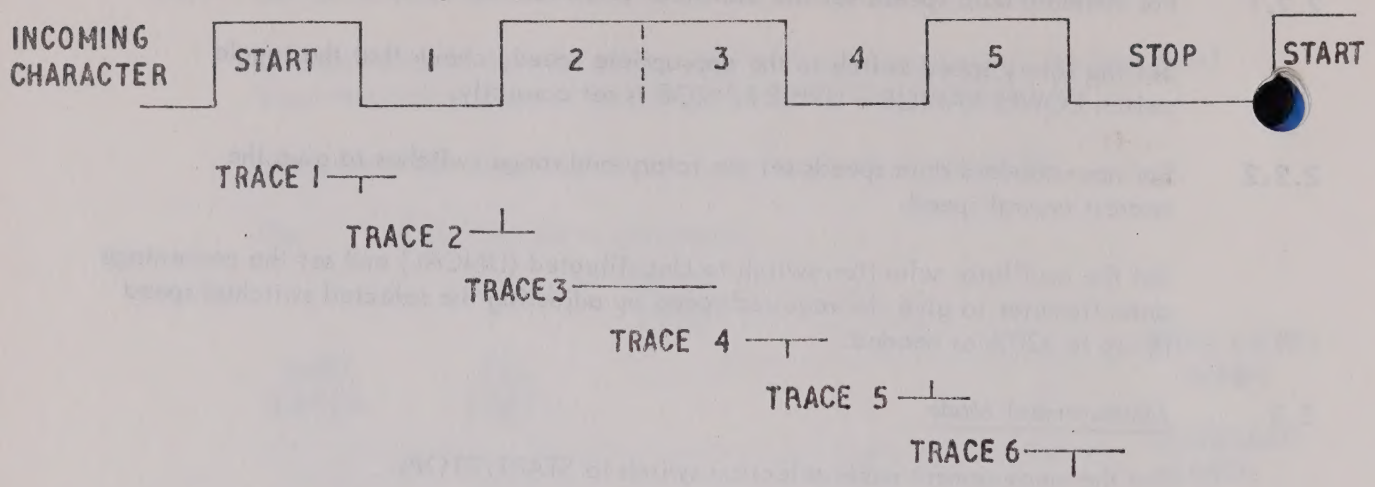


Fig. 4 shows a 5 information e lement code character giving 6 traces, other codes up to 8 element are catered for giving a maximum of 9 traces. The hold peak facility is not available when using the separate element display.

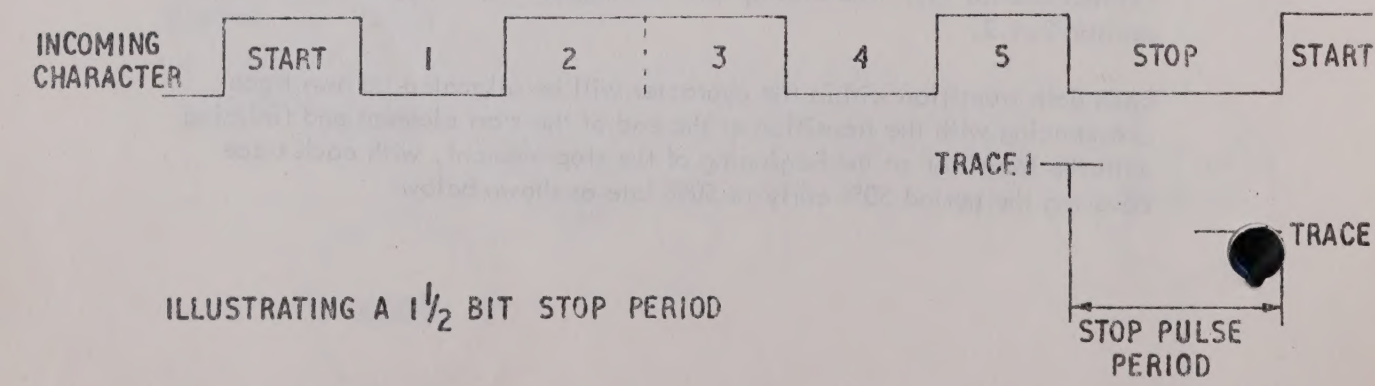
2.4.4 Set the rotary display control switch to INPUT WAVEFORM.

The display will again be triggered by the character start element and the display will include all elements with the exception of the stop pulse, this period being used for the flyback time.

The amplitude of the waveform display can be adjusted by means of a screwdriver slot potentiometer mounted on the rear panel (WAVEFORM AMPLITUDE).

2.4.5 Set the rotary display control switch to STOP PULSE. The display is now triggered half-way through the last information element period in the character and is then continued until the next start element is recorded. Thus the stop pulse period is measured as the time from the transition (or ideal transition time if no transition is present) on the first trace to the end of the display.

Fig. 5 - Stop Pulse Display



ILLUSTRATING A 1½ BIT STOP PERIOD

2.5 Tube Controls

2.5.1 The three potentiometer controls ASTIGMATISM, FOCUS and BRILLIANCE are mounted on the front panel and should be adjusted to suit individual operator requirements.

2.5.2 The HORIZONTAL MAGNIFIER switch control provides four possible displays which are applicable to all positions of the rotary Display Control switch.

2.5.2.1 The X1/0% position gives a display covering the period 50% early to 50% late for distortion and stop pulse displays, centred on the ideal transition time. For the Input Waveform the full character is displayed.

2.5.2.2 The X3/0% position expands the distortion display to cover the period 20% early to 20% late centred on the ideal transition time. For the Input Waveform the centre 1/3 of the character is shown.

2.5.2.3 The X3/30% E position expands the distortion display to cover the period 50% early to 10% early centred on a 30% early position. For the Input Waveform the first 1/3 of the character is shown.

2.5.2.4 The X3/30%L position expands the distortion display to cover the period 10% late to 50% Late centred on a 30% late position. For the Input Waveform the last 1/3 of the character is shown.

2.5.3 The X and Y shift controls are screwdriver slot potentiometers mounted on the front panel.

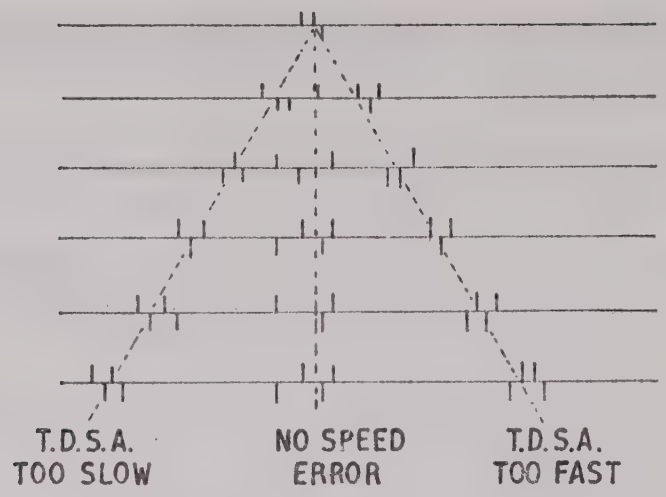
2.6 Threshold Control

For both series and shunt measurements of high level signals a potentiometer threshold is provided on the rear panel. This is a screwdriver slot control calibrated from 5 to 100, and the setting of this control defines the level at which a change in state from Mark to Space and Space to Mark is recognised by the T.D.S.A.

2.7 General

When measuring start-stop distortion the distortion measurements can include distortion due to a speed error, that is if the data source speed is different from the T.D.S.A. speed. This speed error will be apparent when observing the individual element distortions in the 'SEPARATE ELEMENT DIST'N' position. The data transitions will show as a windscreen wiper effect on the display as shown below:

Fig. 6 - 5 Element Character Display



This speed error can be removed by adjusting the T.D.S.A. speed controls to set all of the transitions in an average spread about their ideal times.

3. Free Running Distortion Measurement

When operating in a Free Running Mode the display will run continuously regardless of the type of information being received, i.e. start-stop, or continuous data. It is intended for use with continuous data inputs and will therefore not give sensible answers when used with start-stop data which is not of an end to end character nature.

3.1 Set the Measurement Mode switch to the FREE RUN position. Select the speed range as required, i.e. a switched crystal speed or an UNCALIBRATED speed to adjust the display system to the speed of the incoming data.

In this mode of operation the SEPARATE ELEMENT DIST'N and the STOP PULSE displays will not function correctly, and measurements of distortion can only be taken using the HOLD PEAK DIST'N display.

3.2 General

One useful facility of this Free Run mode is the ability to display the peak distortions received in a block of information, e.g. A short message can be received and monitored in the Start/Stop mode, then the display can be restarted by switching to FREE RUN and flicking the START, +, - switch on the input control, this display will then show the peak distortion recorded during the short message.

4. Synchronous Distortion Measurement

The Synchronous facility is for use with continuous patterns or data streams where every transmitted element is a whole bit period, i.e. half bit stop periods cannot be synchronised. The advantage of the synchronous system is that the display is locked to the incoming data at the correct speed and the distortion spread can easily be seen on the display.

4.1 Set the MODE switch to FREE RUN, adjust the T.D.S.A. speed control until the transition display is close to the correct speed, i.e. the transitions are moving slowly across the screen. Switch the MODE switch to SYNCHRONOUS and the transitions will be locked to an average position about the ideal transition marker on the display.

4.2 General

The accuracy of measurement can be increased by running the receiver at higher speed multiples of the incoming data when operating in a synchronous mode, e.g. if the incoming data rate is 600 bauds and the receiver is run at 2400 bauds then the marker dots will represent $\frac{1}{4}$% steps and not 1% steps.

OPERATING INSTRUCTIONS NOTES FOR T.D.S.A. No.1A ONLY

Error Count

Two count stores are provided within the equipment, each one having a count capability of 999. The outputs from the stores are displayed on the C.R.T. as shown below:

The raster display represents 6 rows of decades from 0 to 9 with the most significant position in each row marked by a double dot. Hence a simple read-out in decimal form is provided as shown in the examples above.

The first store function control switch is mounted on the front panel and the second store control switch is mounted on the rear panel. Both counters are controlled by the three position lever key on the front panel marked as Count, Stop and Reset.

1. Start-Stop Error count

Set the display control switch to 'Error Store'. Set the display mode switch to 'Start-Stop'. Set the speed switch to the data rate and also the input control switches to the correct polarities and character length.

1.1 5 unit Fox Character Errors

In this position the first store will count character errors in the Quick Brown Fox message to I.T.A. No.2. An error being defined as any element transition with a distortion in excess of that set on the Error Threshold switch which is mounted on the rear of the unit. This threshold is adjustable in 5% steps, between 5 and 45%.

An 'In Phase' lamp mounted on the front panel shows when correct phasing is achieved between the incoming data and the internally generated data, thus allowing a comparison for a true error count. The 'In Phase' condition should be achieved before any meaningful error count is made.

1.2 8 unit Fox Character Errors

In this position the first store will count character errors in the 'Quick Brown Fox' message to I.T.A. No.5.

1.3 Parity Errors

This position allows a parity error count for either Odd or Even parity in any 8 unit code start-stop data.

1.4 Q9S Character Errors

In this position the first store will count character errors in the 'Q9S' sequence message to I.T.A. No.2.

2. Synchronous Error Count

Set the display control switch to 'Error Store' and the display mode switch to 'Synchronous'. Set the speed switch to the data rate and the input control switches to their correct positions.

2.1 511 P-R Block Errors

In this position the first store will count the number of 511 bit patterns which are in error. An error is defined as being any element transition which has a distortion greater than that defined by the error sampling switch mounted on the rear panel. This threshold is variable in 5% steps from 5 to 50%.

Before any meaningful error count is made it is necessary to achieve an 'In Phase' condition. This can be achieved in one of two ways. Firstly providing that a correct pseudo random sequence is being received then the in phase condition is achieved automatically when the LINK 1 (AUTO-REPHASE) on Board 5 is connected. If this link is left open then the in phase condition is achieved manually by operating the PHASE button on the front panel.

2.2 511 P-R Element Errors

In this position the first store will count element errors in the 511 bit patterns.

3. Second Store Function

The second store counter is controlled by a rotary switch mounted on the rear of the unit, and the functions and inscriptions are detailed as follows:

3.1 Block Errors/Auto Rephases

In this position the second counter will record block errors in the 511 bit P-R sequence, or, it will record the number of automatic rephasing actions which occur when either of the 'Fox' messages or the 'Q9S' message is being received. An auto-rephase action occurs when 9 consecutive character errors are recorded, the internal message generator is reset and remains so until the phasing character is recognised.

3.2 Blocks/Messages Received

In this position the second counter records either the total number of 511 bit patterns received, or, the number of character messages received, thus allowing error rates to be established.

3.3 Overflow

In this position the second counter acts as as overflow counter for the first counter on any of the first counter functions, thus allowing a total count of 999,999.

TELEGRAPH AND DATA SIGNAL ANALYSER

File: T37

HANDBOOK

APPLICABLE UP TO
SERIAL NO 24006

TREND COMMUNICATIONS
ST. JOHN'S ESTATE
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BUCKS
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PUB NO: TD 410/7/72

QUALITY ASSURANCE
STANDARDS, CALIBRATION, AND
MAINTENANCE LAB.

TELEGRAPH & DATA SIGNAL ANALYSER

HANDBOOK

TYPES 1A AND 2A

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MARCH 1973
ISSUE 2

AMENDMENT No.16 TO TREND PUBLICATION No.426

TELEGRAPH AND DATA SIGNAL ANALYSER TYPES 1A and 2A

Authority: Change Note 2450 Date: 4th June 1974

Items Affected

Mother Board Circuit Fig.2A.

Component List - Mother Board Assembly Section 5.1.

Fig. 2A	R17	delete	1K8	insert	2K2
	R42	"	2K2	"	1K8
	R67	"	47K	"	5K6
	R68	"	5K6	"	47K
	C1	"	10pf	"	47pf

Components List - Insertions and deletions as above plus

C15	delete	10p ±20%	10v	Erie 10 DN
	insert	47p ±10%	5v	Erie HI-K Type YD

AMENDMENT No.17 TO TREND PUBLICATION No.426

TELEGRAPH AND DATA SIGNAL ANALYSER TYPES 1A and 2A

Authority: Change Note 2441 Date: 30 April 1974

Items Affected

EHT Box Fig.9 and Components List Section 5.8.

Fig.9	R3	delete	10Ω	insert 4.7Ω
	C2	"	0.047uF	" 0.1uF
	C10	remove		

Components List Section 5.8

R3	delete	10Ω	insert	4.7Ω
C2	"	0.047 ±20%	30v	Mullard C281
	insert	0.01 ±20%	160v	TFM
C10	delete all reference			

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T.D.S.A. Type 1A only

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T.D.S.A. Type 1A only

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CHAPTER 1

GENERAL DESCRIPTION

The Trend Telegraph and Data Signal Analyser (T.D.S.A.) is a portable, mains-operated instrument for testing tele graph and data transmission equipment. In conjunction with the Trend Telegraph and Data Message Generator (T.D.M.G.) it can be used for assessing the quality of telegraph and data transmission links.

The basic instrument (T.D.S.A. type 2A) provides for measurements of distortion on both start/stop and continuous (synchronous or "isochronous") data streams, which can be received over a wide bit-speed (or baud) range. These measurements can be made in series or shunt with the line being considered, accommodating the wide range of signal levels encountered on telegraph and data transmission equipment. The measurements are represented in the form of self-calibrating lines of dots on a cathode ray tube (C.R.T.). The C.R.T. can also be used to display the actual waveform of the data being measured.

The T.D.S.A. type 1A has all the facilities of the type 2A with the addition that it can be used to make error measurements on the start/stop messages and Pseudo-Random pattern generated by the T.D.M.G. It can also be used for parity checks on any start/stop characters which have "parity bits".

Mechanically, the unit is of robust and rigid construction. The two side panels are aluminium extrusions, as also is the rear panel. The front panel is a plastic injection moulding whilst the top and bottom covers are of black vinyl-covered sheet steel. The carrying handle is attached to the side panels and can be set under the unit to act as a stand. The mains lead is stored in the lid and when in use plugs into the rear panel.

CHAPTER 2

SPECIFICATION AND CONTROLS

2.1 Input Signals

The T.D.S.A. can accept both high level telegraph signals and low level data signals, and measurements can be made in either a shunt mode presenting a high impedance greater than 100K ohms or in a series loop mode, with a series impedance of 18 ohms. The shunt impedance may be switched to 1K ohm if desired.

2.1.1 The high level signals are connected to the upper input socket and referenced to the Telegraph Earth socket. Double current or Single current either polarity can be accepted as determined by the input mode switch.

2.1.2 The low level signal input is connected to the lower input socket and is refernced to the Common socket. This input is a C.C.I.T.T. V24 termination and accepts bi-polar signals in the range 3-25 volts.

2.1.3 The Series/Shunt mode switch is mounted on the rear of the instrument and the type of operation should be selected before any signal is connected to the instrument.

The high level input signals can be up to ±150 volts for shunt measurements or up to ±150mA for series measurements. When operating in a series mode the input is accepted on the high level socket and returned through the Telegraph Earth socket, in this mode the Telegraph Earth socket must not be connected to Protective Earth.

2.1.4 Start Pulse polarity can be selected by the 'Start' toggle switch to accept signals with negative or positive 'Start' polarity.

2.1.5 Amplitude Threshold Control: A calibrated potentiometer control mounted on the rear panel allows transition threshold to be adjusted. The threshold is defined as the point at which a change of state from Mark to Space or Space to Mark is recognised.

The calibration from 5 to 100 indicates volts for shunt measurement and mA for series measurements.

2.2 Speed

Two separate oscillators are provided, the first being a crystal controlled oscillator from which 21 fixed speeds are derived, the second a variable oscillator which allows any speed over the full range to be selected. Selection is by the Cal/Uncal switch.

2.2.1 Crystal oscillator speeds in bits/second.

37.5, 45, 50, 75, 90, 100, 110, 150, 200, 220, 300, 400, 600, 900, 1200, 1800, 2400, 3600, 4800, 7200, 9600.

Accuracy and stability are better than 0.01% and 0.005% respectively.

2.2.2 The variable oscillator is used in conjunction with the range selector switch and allows ±20% variation on any selected switched speed. Thus continuous coverage is provided over the range 30-11, 500 bits/second.

This oscillator has an accuracy of 2% and a long term stability of 1%.

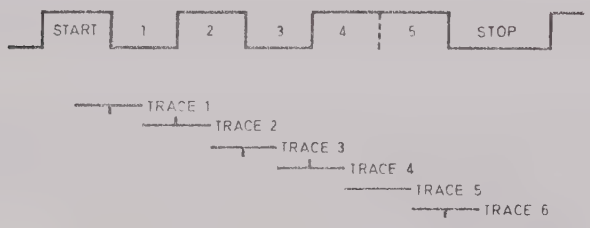
2.2.3 An external timing source can be used to drive the T.D.S.A. This can be at bit rate or 100 times the bit rate required, and is accepted via a socket at the rear of the instrument as described in para.2.7.1.

The type of signal required is:-

a) a rectangular waveform to V24 specification.

b) a rectangular waveform 0 to +5V.

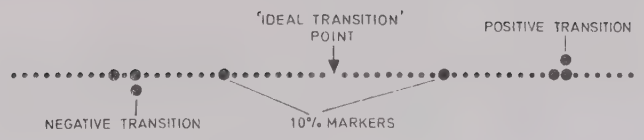
2.3.1 Start/Stop information is generated on a character by character basis, and the receiving equipment is prepared to receive each character by the recognition of a start element. Measurement must therefore be referenced to the leading edge of each start element. Distortion is defined as the displacement of a transition from the ideal instant expressed as a percentage of the information element. The T.D.S.A. inspects each transition over a range covering 49% early to 49% late, about the ideal transition point and these transitions are displayed on self calibrated horizontal trace displays.



Diag. 1

Diag.1 shows a typical 5 unit coded character with single bit start element and a $1\frac{1}{2}$ bit stop element. The diagram also shows the time relationship of the 6 "distortion display" traces, relevant to the 6 possible "transition positions", which are brought up on the C.R.T.; a 6 unit character would have 7 traces and so on, as selected by the Elements Per Character switch.

Each trace is made up of a horizontal line of marker dots representing the 98 one-percent divisions between 49% early and 49% late. The ideal or zero distortion point is identified by the absence of a dot in the trace centre, whilst, starting from the centre each tenth dot is brightened to denote the 10% points. Transitions are displayed by the presence of a dot above or below a marker dot, representing positive or negative transitions respectively. (See Diag.2).



Diag. 2

2.3.2 The Display Control switch selects the type of display as detailed below:

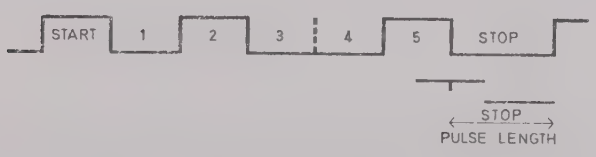
2.3.2.1 Hold Peak Distortion: With this display all of the traces are superimposed on each other and a collective distortion display is provided. The main facility in this position is the ability to store, update and display continuously the peak values of distortion measured for both Early and Late readings. The stores will hold the highest value of distortion received until manually reset by operation of the push button switch below the display control switch.

2.3.2.2 Separate Element Distortion: This display provides a vertical separation of the traces described above thus allowing inspection of each individual element distortion.

It is also possible to observe and measure speed error by utilising this method of display.

2.3.2.3 Input Waveform: The actual input signal waveform is displayed thus allowing observations to be made of rise and fall times and possibly contact bounce where relays are employed. To facilitate the latter, when the display is expanded as described in para.2.4, bright "dots" are superimposed on the waveform at intervals of 10% of a signal element.

2.3.2.4 Stop Pulse: To measure this period, the distortion display is started in the centre of the last information element and continued until the next start element is detected, thus the length of the display from the last information transition time to the end of the total display is a direct measurement of stop pulse length. Diag. 3 gives an example of a 5 unit code character with a $1\frac{1}{2}$ bit stop period.



Diag. 3

2.4 Synchronous Distortion Measurement

The synchronous measurement facility is used to measure distortion in continuous data streams, e.g. any of the standard line test patterns 1:1, 2:2, 511 bit pseudo-random patterns etc. The display is similar to that for Start/Stop Distortion Measurement (para. 2.3), with the exception that there is only one distortion trace even though the display control be set to Separate Element Distortion.

A synchroniser in the T.D.S.A. establishes a timing reference against which measurements are made. Synchronisation to any of the 'Cal' (fixed) speeds available on the T.D.S.A. is automatic when the Start/Stop-Free Run-Sync switch is set to 'Sync', but operation to a speed which is only obtainable by the Variable Oscillator is as follows:-

With the 'ST/ST-Free Run-Sync' switch set to Free Run the receiver speed is set to the nominal bit rate and the Display Control to Hold Peak Distortion. The transitions will then drift across the display and the Variable Oscillator control can then be adjusted to give a very slow rate of transition drift.

Once this condition is achieved switch to Synchronous and the transition display will be locked about the ideal transition time on the display. A lamp indication on the front panel shows when the synchronised condition is achieved. The values of Peak Early and Late distortion will give a true value isochronous distortion.

When operating in a synchronous mode the Stop Pulse 'Display Control' position is not applicable, also the 'Separate Element Distortion' position gives a single horizontal trace without 'hold peak' transitions.

If a loop check is to be made on a system e.g. 'back-to-back' Modem then by employing a T.D.M.G. and a T.D.S.A. a common timing source can be used for both. This means that an absolute measurement distortion can be obtained when compensation for the delay between transmitter and receiver has been made. To do this the T.D.S.A. Speed Control is set to 'Ext' and the 100 times bit rate output signal from the T.D.M.G. used to drive the 100 times bit rate input on the T.D.S.A. back panel (see 8.1 - Ancillary Input/Output). The T.D.S.A. Start/Stop-Free Run-Sync switch is now set to 'Sync' to align the T.D.S.A. with the incoming data. When this is achieved (i.e. transitions are occurring equally spaced around the ideal transition point) the T.D.S.A. is set to 'Free Run'. This will disable the synchroniser, so that the T.D.S.A. retains a fixed reference for incoming data transitions.

2.5 Tube Controls

The standard C.R.T. display controls are provided on the front panel for Focus, Brilliance and Astigmatism. A Horizontal Magnifier switched control is also included to expand the display. This 4 position switch gives the following expansions:

a) 0% X 3. The distortion display in this position gives a coverage from 49% Early to 49% Late, with the trace centre at the zero distortion point. On Input Waveform, the whole character will be displayed.

b) 0% X 3. The distortion gives a coverage from 19% Early to 19% Late centred on the zero distortion point. On Input Waveform, the middle period only of the character will be displayed, magnified by 3.

c) 30% X 3. The distortion display gives coverage from 49%Early to 10% Early centred on the 30% Early point. On Input Waveform, the first part of the character will be displayed, magnified by 3.

d) 30% X 3. The distortion display gives coverage from 10% Late to 49% Late centred on the 30% Late point. On Input Waveform, the last part of the character will be displayed, magnified by 3.

2.6 Error Count

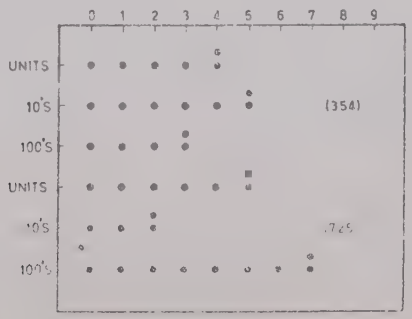
The error count system operates comparing the incoming data stream with an internally generated message or pattern and any discrepancies are defined as errors. The incoming patterns and messages must be the same as those generated within the T.D.S.A., as provided by the Trend T.D.M.G.

A pattern phase relationship must be correctly established to enable error detection, the phasing cycle within the T.D.S.A. being initiated by the 'Phase' push button. A lamp indication shows when the correct pattern phase is achieved. An automatic phasing action is initiated for the Start/ Stop messages if nine consecutive characters are in error.

Element errors are defined as an incorrect comparison at a predetermined sampling time during the element period. The sampling points are selected by a switch mounted on the rear panel and can be switched in 5% steps from 5% to 45% through the element period for all patterns. For the 511 bit P-R pattern, it is also possible to sample at the 50% point.

A display of the error counters results by setting the Display Control to Error Store.

The display is shown on the C.R.T. as 6 rows of dots with each row containing up to 10 dots and thus representing a decade (see diagram). The most significant dot in each row is emphasised by a dual dot display. The count capacity is up to 10^6. This can be split to give two separate counters of up to 10^3 capacity each. By this means error rates can be established by counting errors in the first store and total information received into the second store.



Diag. 4

The Error Count Control switch allows the following types of error to be detected and displayed.

a) 5 unit Fox Character Error: In this position the error store counts every character which is in error during the 5 unit code (I.T.A. No.2) 'Quick Brown Fox' message as generated by the T.D.M.G.

b) 8 unit Fox Character Error: Character errors are detected in the 8 unit code (I.T.A. No.5) 'Quick Brown Fox' uppercase, even parity as generated by the T.D.M.G.
For both (a) and (b) a character is defined as being in error if one or more elements in the character are incorrect at the sampling time.

c) Parity Errors: For parity coded start/stop characters, errors can be counted for either Odd or Even parity.

d) 511 bit Pseudo-Random Pattern Errors: The error store can be set to count either element errors in the pseudo-random sequence, or block errors, which are full pseudo-random patterns of 511 bits which have one or more elements incorrect.

e) 'Q9S' Character Errors: Character errors can be counted in the Q9S message to C.C.I.T.T. recommendation R51.

The second error store control switch is mounted on the rear panel and controls the following store functions:

f) Overflow: This position places the second store in series with the first error store to provide 10^6 count capacity.

g) Block/Auto rephase: When using the first store as described in (d), then the second store counts pseudo-random block errors. When using the first store as described in (a), (b) and (e) then the second store counts the number of automatic rephasing actions.

h) Block/Messages Received: In this position the second store counts the total number of pseudo-random blocks or Fox messages or Q9S messages received.

i) Both error stores are under the control of the three position Count-Stop-Reset switch on the front of the unit.

2.7 Ancillary Controls

Certain facilities can be supplemented or modified by a control panel mounted at the rear of the instrument.

Control is affected by insertion or omission of 'U' links between two columns of sockets on the panel.

a) External Element Timing: By insertion of a link the T.D.S.A. can count errors in the 511 bit Pseudo-Random Pattern when using an external element rate timing source. (e.g. synchronous modem clock). For this mode of working the 'Speed Bits/Sec' switch should be set to any position other than 'Ext".

b) Hold Max. Pos. & Neg. only: By insertion of a link positive or negative transitions respectively are held in the peak distortion stores.

A potentiometer mounted on the rear of the instrument enables the amplitude of the 'Input Waveform' display to be varied.

2.8 Ancillary Input/Output

Provision is made on the rear of the instrument for the input and output and monitoring of certain useful signals.

2.8.1 Sockets are provided on the panel for:

a) Input timing source at 100 times bit rate. This signal is required to be at logic (0 to +5V) or CCITT V24 level (In 100x Clock).

b) Output timing at 100 times bit rate at logic level (Out 100x Clock).

c) Input of Element Timing Signal with level as on (a) (Timing Element In).

d) Output of an element timing signal producing one cycle per element at logic level. (Timing Element Out).

e) Output of a Character Timing signal producing a pulse which is low from the mid-point of the start element until the middle of the stop elements (5, 6, 7 unit characters) or the middle of the 8th information element (8 unit characters) at logic level (Timing CH).

f) Output of Message timing signal producing a pulse of 1/100 of an element in width per message at logic level (Timing Mess).

g) Output of Pseudo-Random block signal producing a positive pulse one element in length per 511 bit sequence at logic level (Timing Block).

h) The two bottom sockets on the panel provide the 0V (Signal Common) connection to which all the signals on the panel are referred.

2.8.2 A 25-way socket is provided to give access to the following:

Pin No.	Signal	Function
1	0V	Common Return
2	Received Data (Out)	Data normalised to logic level 0V=1, +5V=0.
3	Sig.El.Timing (Out) -% Dist.Counter Early/Late	1:1, positive transitions coincident with ideal data transitions. 0V during 'Early' +5V during 'Late'.
4	% Dist.Counter,BCD 1 +5V=1, 0V=0	
5	% Dist.Counter,BCD 2 +5V=2, 0V=0	
6	% Dist.Counter,BCD 4 +5V=4, 0V=0	Used in conjunction with Dist'n. Read-out Timing (pin 11) gives % distortion of transitions.
7	% Dist.Counter,BCD 8 +5V=8, 0V=0	
8	% Dist.Counter,BCD 10 +5V=10, 0V=0	
9	% Dist.Counter,BCD 20 +5V=20, 0V=0	
10	% Dist.Counter,BCD 40 +5V=40, 0V=0	
11	Distortion Read-out Timing	Negative going pulse, 0V and +5V, 1% of element per transition.
12	Element Error Pulse	Positive pulse, 0V and +5V per element in error in the Pseudo-Random sequence.
13	Block Error Pulse	Positive pulse, 0V and +5V per 511 bit block in error in the Pseudo-Random sequence.
14	Parity Error Pulse	Positive pulse, 0V and +5V per parity error in start/stop characters.
15	Character Error Pulse	Positive pulse, 0V and +5V per character error in Fox and Q9S messages.
16	Block Timing	Positive pulse, 0V and +5V see 2.8.1.(g)
17	Character Timing	Positive pulse, 0V and +5V see 2.8.1.(e)
18	Message Timing	Positive pulse, 0V and +5V see 2.8.1.(f)
19	100 x Clock Out	0V and +5V. see 2.8.1.(b)
20	Rephase Control (In)	0V to rephase, O/C or +5V normal.
21	100 x Clock In	See 2.8.1.(a)
22	Element Timing I/P	See 2.8.1.(b)
23	V24 Data (In)	Data Input
24-25	Not Used	

2.9 Operational Conditions

The instrument is designed to operate over a temperature range of 2°C to 40°C ambient and in a relative humidity between 40 and 90% ambient. All preset adjustments are made during manufacture and consequently no field calibration is necessary other than the C.R.T. display controls provided.

2.10 Mechanical

The unit is fully self contained and of rugged construction suitable for field use. The T.D.S.A. can be mounted together with a Trend Telegraph and Data Message Generator (T.D.M.G.) in a 19 inch rack. The rack mounting adaptor is available as an optional extra.

2.10.1 The T.D.S.A. dimensions are as follows:

Height	6 inches	15cms
Width	9 inches	23cms
Depth	18 inches	46cms
Weight	25 lbs	11.4kgs

2.10.2 The unit has an attractive two tone finish in black and silver grey.

2.11 Power Connections

The mains is connected by a 3 pin socket mounted on the rear panel. Each unit is provided with an 8ft mains cable with colour code conforming to the European standard.

The unit can operate with mains input 50 to 60Hz and with voltages in the ranges 190 to 250V or 95 to 125V. The appropriate tap setting is achieved by means of a voltage selector mounted on the rear panel. A 1A delay type fuse link is required for 240v, or a 2A link for 115v.

2.12 Model Variants

Two models of the unit are available:

T.D.S.A. No.1A: This model has all the facilities described.

T.D.S.A. No.2A: This model has none of the error count facilities. The 25 way socket described in 2.8.2 is also omitted.

CHAPTER 3

CIRCUIT DESCRIPTION

3.1 General

3.1.1 Start/Stop Distortion Measurements

In order to make measurements to an accuracy of 1% it is necessary first to provide a system clock at 100 x the element rate of the data stream to be measured. This clock is normally derived internally from one of the two 2.88MHz oscillators via the Speed Divider which is switched by the SPEED BITS/SEC switches to give the required frequency, although an external 100 x element rate signal can be used if required.

The selected 100 x element rate clock, HSS, drives a binary-coded decimal (b.c.d.) 50-way Up/Down (or Reversible) Counter. When the counter is allowed to run, the Up/Down Control causes the counter to count from 0 to 49 in the Up mode followed by 49 to 0 in the Down mode and so on, the result being a total count of 100 with the Up/Down Control (a bistable) switching at element rate. The element rate signal thus obtained is used to drive the 6-9-way binary Character Length Counter.

The purpose of the Up/Down Counter is to divide the elements of the incoming characters into one-percent divisions. The Character Length Counter is used to define the element transitions of the character, i.e. Start Elements - 1st Info. Element transition, 1st Info. Element - 2nd Info Element, etc., up to Last Info. Element - Stop Element transition. The count length of the Character Length Counter thus depends on the number of elements per start/stop character as selected by the ELEMENTS PER CHARACTER switch.

Control is exercised over the Up/Down and Character Length counters by the Start/Stop Control, such that when start polarity is detected at the Received Data Input Circuit, the counters are allowed to run for the duration of one character. The Short Start Reject Circuit ensures that if a supposed start signal turns out to be only a noise spike, then the counters will be reset and remain so until the next start polarity is detected.

The binary Character Length Counter stages are fed to a Digital-to-Analogue converter circuit, the output of which controls the Y deflection circuit of the C.R.T. to give the vertical positions of the 6-9 calibrated horizontal traces relevant to start/stop distortion measurements. The X deflection of each trace is obtained using a "Pump" circuit, which is driven by the 100 x element rate clock; this moves the trace horizontally across the tube face in "one-percent" increments giving a display of one-percent "dots". The middle dot is "blanked out" to indicate the centre or "0%" part of the trace whilst every tenth dot (counted from the "0%" point outwards in both directions) is "brightened up" to accentuate the "10%" markers.

3.1.1 continued

The detection of transitions on input data, accomplished in the Input Data Retiming circuit, is used to modify the Y deflection and at the same time increase the trace brightness to give the required indication on the display. The effect of this is to provide a small positive deflection of one of the trace's one-percent dots when a positive transition is detected and a negative deflection for a negative transition, the position of this deflection relative to the "0%" or "ideal transition" point giving the distortion present on that transition, e.g. a deflection 11 dots to the left of 0% on a trace indicates a transition distorted "11% Early".

The "Hold Peak Distortion" Store is used to hold those states of the Up/Down Counter which correspond to the early and late transitions of input data that occur farthest away from the "ideal transition" point. The output from this store is used to feed in "hold peak transitions" to the tube display Y Scan and Brightness circuits, alongside the actual transitions detected in the Input Retiming Circuit.

3.1.2 Isochronous Distortion Measurements

Isochronous measurements will normally be made with the START/STOP-FREE RUN-SYNC switch in the SYNC position. In this situation, unlike the START/STOP setting, the Up/Down Counter will run continuously after detecting the first start polarity signal. The Phase-Locking Circuit will "advance" or "retard" the counter as appropriate (by making the count 101 or 99 respectively), in an attempt to line up the counter's zero point with the incoming data transitions. In practice when phase-locking to distorted transitions, the counter's zero point will be lined up with the "average" transition position.

The display of actual and "held peak" transitions is performed in a similar manner to that for Start/Stop working, but only one trace of "marker dots" is produced even in the SEP ELEM DIST'N position of the DISPLAY CONTROL switch as more would be irrelevant.

Operation when switched to FREE RUN is the same as for SYNC, except that the Phase-Locking Circuit is disabled. This can be used for measuring the distortion present on Start/Stop "Blocks" of data.

3.1.3 Error Measurement (T.D.S.A. 1A only)

Character errors will be dealt with first. The Character Length Counter drives the Message Length Counter which has a length of count determined by the message selected on the ERROR COUNT CONTROL switch. The M.L. Counter is used to address the Read-Only Memory, which contains the Q9S and two Fox messages. When a phasing sequence is initiated, the M.L. Counter is held in its zero state by the Start/Stop Message Phasing Control until an incoming character agrees with that held in the R.O.M. When this has happened the M.L. Counter is allowed to step, but if 9 consecutive character errors are detected sometime later, an "out-of-phase" condition will be considered to exist and a new phasing sequence initiated.

3.1.3 continued

Parity errors are detected in the Parity Error Detection circuit by generating a "local" parity bit and comparing it with the actual parity bit received.

Errors can also be detected in the standard 511-bit Pseudo-Random sequence. This is done by first aligning the local Pseudo-Random Generator by means of the P-R Phasing Control and thereafter comparing the locally generated pattern with that being received. For such a measurement the instrument is normally run in the SYNC mode. Also available is the facility to use an EXTERNAL ELEMENT TIMING signal, e.g. for use with a Synchronous Modem which supplies its own timing.

There are two 3-decade Error Counters which can be used for the purpose of recording errors detected, number of start/stop messages received, number of automatic rephasing operations, etc. The display on the tube consists of 6 horizontal lines of up to 10 dots, where each line represents one of the counter decodes and the number of dots in the line represents the count (from 0-9) in that decode. These lines of dots are basically the distortion display traces where all but the "5%" dots have been "blanked out". For each line the Error Display Control causes the dot representing the "significant digit" of the associated counter to be given a deflection similar to that for a positive transition in the distortion display, whilst the rest of the line is held blanked out.

3.2 Logic Elements

3.2.1 General

The digital integrated circuits used in the instrument consist of 3 types:

Fairchild "930" series gates and bistables;
Fairchild "9300" type M.S.1. circuits;
National Semiconductors type "MM5220" M.O.S. Read only Memory (R.O.M.)

They are represented in the circuit diagrams by B.S. symbols or in the case of the more complex functions by a rectangle.

Circuits are numbered as follows:

Gates have the circuit reference number written in the middle of the symbol and the relevant pin numbers by their inputs and outputs. The circuit type number (e.g. "962" for a 3 input gate) is written by the symbol.

Bistables are treated in a similar manner to gates, but as the symbol is larger the circuit type number is written inside with the circuit reference number. Also written inside is the name of the bistable, e.g. "MUP" in bistable IC.13(1-6) on Fig.3.

The "9300" elements and R.O.M. are treated similarly with the addition of abbreviated titles for the pin functions.

3.2.2 NAND Gates (936, 946, 962, 930, 932 on Fig. 13A)

All gates perform the 'positive logic' NAND function, i.e. when all inputs to a gate are positive (logical '1' or MARK state) the output is at 0v (logical '0' or SPACE state); under all other input conditions the gate is positive. With the 930 and 932 elements it is possible to expand the number of gate inputs by using the nodes available on pins 3 and 11. The 932 element is used where a large "fan out" is required.

A feature of all gates except the 932 is that several gate outputs can be joined together in the 'wire OR' configuration; with this arrangement any gate whose inputs are all high will hold the common output point low, i.e. all gates have to have at least one input low for the common output to go high.

3.2.3 Bistables (9093 on Fig. 13A)

The bistables are of the d.c. triggered, J-K master/slave type. With this type of circuit, data is fed into the master (or input) bistable whilst the clock waveform is high. When the clock goes low, the slave (or output) bistable will take up the state of the master bistable. The Sd input can be used to switch the circuit asynchronously and over-rides the clocked inputs.

The drawing convention used in the circuit diagrams is such that the bistable 'set' input and 'true' output are always considered to be the top pair of input/output connections on the symbol, e.g. in Fig.3 and for bistable MUP (IC.13(1-6) the set input is pin 3 and true output ("MUP") is pin 6 whilst the reset input is pin 2 and the inverse output ("$\overline{\text{MUP}}$") pin 5. Also, in this case, the asynchronous input on pin 4 is used to set the bistable, as taking pin 4 low will force pin 6 high.

3.2.4 Up/Down Counters (9306 on Fig. 13A)

The 9306 is a synchronously presettable, reversible, 10-way binary coded decimal (b.c.d.) counter made up from 4 bistables, the outputs of which represent each counter state in "weighted" code, i.e. Q0 = 1, Q1 = 2, Q2 = 4 and Q3 = 8 so that state 3, for example is represented by $Q0.Q1.\overline{Q2}.\overline{Q3}$.

If the 'counter enable' inputs CE are all high and the 'count direction' input CD is also high, then application of clock pulses to clock input CP will cause the counter to count "up", 0, 1, 2, 3, 4, 5, 6, 7, 8, 9,0, 1, 2, etc. giving a "terminal count" output TC on each count of 9. If CD is low, then the counter will count "down" 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, 9, 8, etc. giving output TC on each count of 0.

3.2.4 continued

If "parallel enable" input PE is taken to 0v, CE will be over-ridden and the counter stages set to the states corresponding to the conditions imposed on inputs P0 - P3 under the control of clock input CP.

The clock required to drive the counter is the inverse of that required to drive a "9093" type of bistable; data is fed into the counter whilst the clock is low and the counter stages change state immediately after the clock goes high.

3.2.5 B.C.D. Decade Counter (9310 on Fig. 13B)

The 9310 is a synchronously presettable, 10-way binary coded decimal (b.c.d.) counter made up from four bistables, the outputs of which represent each counter state in "weighted" code, i.e. Q0 = 1, Q1 = 2, Q2 = 4 and Q3 = 8. State 3, for example, is represented by $Q0.Q1.\overline{Q2}.\overline{Q3}$.

If the count enable inputs CEP and CET are both high, and if the parallel enable input PE is also high, application of clock pulses to clock input CP will cause the counter to count 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, 1, 2, etc., giving a terminal count output TC on each count of 9. If CEP is low, counting is inhibited. If CET is low, counting is inhibited and TC held low regardless of the count.

If the parallel enable input PE is taken low, the counter stages will be set to the states corresponding to the condition imposed on inputs P0 - P3 under the control of clock input CP.

When the asynchronous master reset input MR is taken low, the counter will be reset to the "count 0" state, regardless of the other input conditions.

The clock required to drive the counter is the inverse of that required to drive a "9093" type of bistable; data is fed into the counter whilst the clock is low and the counter stages change state immediately after the clock goes high.

3.2.6 Dual 4-Bit Latch (9308 on Fig. 13B)

The 9308 consists of two separate 4-bit latch sections which provide parallel gated data storage. Each section has four outputs Q0, Q1, Q2, Q3, an over-riding master reset MR and a two-input active low AND enable.

Data enters a latch when both enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs go high, the data present in the latch at that time is held in the latch and is no longer affected by the data input. The active low master reset over-rides all other input conditions and when activated forces the outputs of all the latches low.

3.2.7 5-Bit Comparator (9324 on Fig. 13B)

The 9324 is an expandable comparator which provides comparison between two 5-bit words A0 - A4 and B0 - B4, and can give one of three outputs, "less than" A< B, "greater than" A>B and "equal to" A=B. A high level on the active low enable inputs E forces all three outputs low.

Words of more than 5 bits are compared by connecting 9324 comparators in series; this is done by connecting the A>B and A<B outputs of the first 9324 to the A0 and B0 inputs respectively of the next stage.

3.2.8 Eight-Input Multiplexer (9312 on Fig. 13B)

The 9312 is an 8-input multiplexer which can select one bit of data from up to eight sources I0-I7. It has complementary outputs Z and $\overline{Z}$, active low enable E and internal select decoding. When E is high, output Z is low and $\overline{Z}$ high regardless of the other input conditions. Data is routed from one of the inputs I0-I7 to the outputs according to the three-input binary code applied to the select inputs S0 - S2.

3.2.9 Read-Only Memory and Drivers (MM5220 and DM8810 on Fig. 13A)

The MM5220 is a 1024-bit static read-only memory (R.O.M.), the contents of which are customer-specified, being inserted during one stage of the device fabrication. The output can be obtained either in the form of 256 x 4 bit or 128 x 8 bit parallel words, under the control of the MODE CONTROL input; for the T.D.S.A., "128 x 8" operation is required and to obtain this the MODE CONTROL and A8 inputs are taken to a permanent 0v as shown in Fig. 3. VDD is also taken to 0v whilst VSS is taken to +15v and VGG to -15v. The R.O.M. is a "negative logic" device, i.e. a '1' is a more negative level than 1 '0' and with the aforementioned supply voltages a level on the A1 - A8 (binary address), MODE CONTROL or CHIP ENABLE inputs is considered to be a '1' between 0v and +4v and a '0' if between +10v and +15v. These high level signals are obtained by using DM8810 high level driver circuits, which are 2-input NAND gates with "free O/P collectors" capable of switching at +15v.

"CHIP ENABLE" is gated into the parallel outputs B1 - B8 and when at 0v will allow the outputs to take up the states of the 8-bit word selected by the binary address inputs A1 - A7. When CHIP ENABLE is high, B1 - B8 will remain low.

The truth table for the R.O.M. used in the instrument (MM5220 GJ) is given below. Address 0 is given by $\overline{A1}.\overline{A2}.\overline{A3}.\overline{A4}.\overline{A5}.\overline{A6}.\overline{A7}$, address 1 by $A1.\overline{A2}.\overline{A3}.\overline{A4}.\overline{A5}.\overline{A6}.\overline{A7}$, and so on. It must be rembered here that this is "negative logic", unlike the rest of the logic in the instrument, therefore a '0' output as given by the truth table is seen as a '1' by the "positive logic" circuits it drives and a '1' is seen as a '0'.

3.3 Detailed Description

3.3.1 Oscillators and Dividers (Fig.3)

The 100 x bit rate clock (HSS) required for operation of the T.D.S.A. is obtained from one of two 2.88MHz oscillators, followed by a divider chain which is conditioned by signals from the SPEED BITS/SEC switch SW9 to give the required division for the speed selected.

The 100 x bit rate clock obtained at the output of the Dividers is "frequency doubled" and the result "divided-by-two", thus giving the final 100 x bit rate clock HSS; this "divide-by-two" action is modified under the control of the Start/Stop Control to improve measurement accuracy.

The oscillators used are a fixed (crystal controlled) oscillator for use when precise setting of speed is required and a variable oscillator for use when checking start/stop synchronous distortion (speed error removed) or setting a speed not given directly by SW9.

3.3.1.1 Crystal Oscillator (Fig.3)

This is a straightforward Colpitts oscillator, transistor TR1 being the oscillating transistor. The collector of TR1, which takes no part in the oscillator action itself, is taken to the base of the buffer transistor TR2 from the collector of which the output is taken. Transistors TR10 and TR11 are used to inhibit oscillation when the Variable Oscillator is being used.

3.3.1.2 Variable Oscillator (Fig.3)

This is an emitter-coupled, emitter-timed oscillator. TR5 collector, which has no part in the action of the oscillator, provides a signal to drive transistor TR7 which in turn drives the output transistor TR8. Transistors TR4 and TR6 provide constant currents for the oscillator transistors TR3 and TR5, to give linear ramps on the emitters of TR4 and TR5 and thus make the switching points well defined. The amplitude of these ramps is controlled by the resistor RV6 in the collector of TR3, which is variable by ±20% at the front panel.

3.3.1.3 Oscillator Selection (Fig.3)

IC's.20(1,2;9,8) and 12(1,2,3) are used under the control of the CAL/UNCAL switch SW10 (Fig.10) to decide which of the two oscillators is to be employed. If SW10 is in the CAL position, signal $\overline{\text{CAL}}$ is low and the output of the crystal oscillator (TR2 collector) is allowed to switch IC.20(1,2) and hence drive the dividers as IC.20 pin 9 is low; in this situation IC.12 pin 2 is also low and thus inhibits the effect of the variable oscillator (TR8 collector). With SW10 in the UNCAL position, $\overline{\text{CAL}}$ and hence IC.20 pin 9 is high and pin 8 will hold the crystal oscillator output low; IC.12 pin 2 will now be high and therefore allow the variable oscillator to switch IC.12(1,2,3) and hence the divider. A further effect in this switch position is that the crystal oscillator is prevented from oscillating via transistors TR11 and TR10.

3.3.1.4 Speed Divider (Fig.3)

The SPEED BITS/SEC switch SW9 (Fig. 10) applies signals ($\overline{9600}$, $\overline{7200}$, $\overline{4800}$ etc.) to condition the divider chain to give the output frequency required. $\overline{9600}$ will only be low when SW9 is set to 9600 bits/sec, $\overline{7200}$ low for 7200 bits/sec and so on down the range. $\overline{EXT}$ is low when SW9 is switched to EXT, when an external timing signal of 100 x the required bit rate (EXT TIM I/P) can be injected via transistor TR9.

Bistables MD1 and MD2 (IC's.11(1-6) and 10(1-6) respectively form a divider which can divide by either 3 or 4, depending on the state of the signal on IC.19 pin 4. If this signal is low (obtained with speeds of 7200, 3600, 1800, 900, 90 and 45 bits/sec), IC.19 pin 6 and therefore MD1 input IC.11 pin 2 will always be high and the divider will divide by 4. If the signal on IC.19 pin 4 is high, however (i.e. all speeds other than those just listed), the signal appearing on IC.11 pin 2 will be identical to that on IC.10 pin 6 and the divider will divide by 3. The output of this stage (IC.10 pin 8) drives a binary divided by 4 stage, MD3 and MD4 (IC's. 10(8-13) and 9(1-6)).

On all speeds other than 110 and 220 bits/sec, IC.19 pin 10 is high and therefore allows MD4 (IC.9 pin 6) to switch IC.19(10,9,8) and hence the clock input (IC.9 pin 13) to the divide by 2 stage, MD5. If either of these two speeds is selected, however, IC.19 pin 10 goes low and IC.25 pin 5 goes high; the signal which is now fed through to the clock input of MD5 is effectively the 2.88MHz oscillator square wave minus every twelfth positive excursion. This is obtained by decoding one of the states of the first two dividers, which are arranged to divide by a total of 12. This decode, obtained on IC.24(3-6), is applied to IC.25 pin 1 to inhibit every twelfth pulse of the 2.88MHz oscillator present on IC.25 pin 4. This action reduces the effective frequency of the signal presented to the clock input of MD5 by a twelfth to 2.64MHz, thus enabling the 100 x bit-rate clock for 110 and 220 bits/sec working (i.e. 11 and 22KHz respectively) to be obtained by subsequent normal division, which would not have been possible with the original frequency of 2.88MHz.

Bistables MD6, MD7 and MD8 (IC's.8 and 1(1-6)) may be arranged to divide by 5,6 or 8. If IC.12 pin 13 is high and IC.19 pin 12 low (speeds 400,220, 100 or 50 bits/sec) then the signal on MD5 input IC.8 pin 2 will be the inverse of that on IC.8 pin 9 and MD6 and MD7 will act as a divide by 3. The "ANDed" combination of MD6 and MD7, obtained via IC.17(9,8), is used to drive MD8, which gives a further division by 2 and thus a total division for the stage of 6. If IC.19 pin 12 is high and IC.12 pin 13 low (speeds 7200,3600,1800,900,220,110,90 or 45 bits/sec) the signal on MD6 input IC.8 pin 3 will be the "ORed" combination of MD7 and MD8, thus making the whole stage divide by 5. If the signals on IC.19 pin 12 and IC.12 pin 13 are both low (all other speeds than those just mentioned) then the bistables will divide by 8.

3.3.1.4 continued

Bistables MD9 and MD10 (IC's.1(9-13) and 2(1-6)) may be arranged to divide by 3 or 4. If IC.16 pin 3 is high (speeds 110 or 220 bits/sec) then the signal on MD9 input IC.1 pin 12 will be identical to that on IC.2 pin 6 (MD10) and the divider will divide by 3. If IC.16 pin 3 is low, however (all speeds other than 110 or 220 bits/sec) then MD9 input IC.1 pin 12 will be permanently high and the divider will divide by 4.

Bistables MD11 - MD13 (IC's.2(8-13) and 3) will always act as a divide by 8.

Selection of the appropriate divider output for each speed is accomplished in the "Divider Output Selection" gates.

3.3.1.5 Final High Speed Clock Phase Adjustment (Fig.3)

To improve the measurement accuracy of the instrument, HSS (the 100 x bit rate clock) is arranged to go to its low level state immediately each new start element has been detected. This is accomplished by taking the initial 100 x bit rate signal on IC.26 pin 11, forming narrow negative pulses coincident with each transition on that signal and applying the resultant 200 x bit rate signal to the bistable MHS. The latter divides by two to produce the final version of HSS. MHS is reset via its asynchronous input every time a new start element is detected, i.e. every time MS1, the Start/Stop Control bistable (section 3.3.5) becomes set.

IC's.25(8-11;1,2,13,12), 26(1,2,13,12), 27(1,2;5,6) and 14(1,2) comprise the "narrow pulse forming" circuit, together with C9 and C10, which derives the clock input to MHS. IC.30(1,2;3,4;11,10;13,12) and C11 are used to form a narrow negative pulse to reset MHS via the asynchronous input on IC.11 pin 10, whenever MS1 becomes set, as detected by $\overline{MS1}$ on IC.30 pins 11 and 13 going low. $\overline{MHS}$ drives IC.29(8-13) to provide HSS and $\overline{HSS}$ is formed on IC.29(1-6).

3.3.2 50-Way Up/Down Counter and Up/Down Control (Fig.3)

The b.c.d. 50-Way Up/Down Counter is driven by the 100 x element-rate clock HSS. Its purpose is to define the 1% divisions of each incoming data element from 49% "Early" to 49% "Late" relative to the "ideal transition" point, the Up/Down Control giving the Early/Late indication. When allowed to run, the counter counts 0-49 "up" from the "ideal transition" time to the "ideal" mid-point of a data-element period and 49-0 "down" from the ideal mid-point to the ideal transition time. Any data transition detected during the "down" half-cycle is considered to be "Early" and one detected during the "up" half-cycle is considered to be "Late", the b.c.d. state of the counter at the instant of transition detection giving the magnitude of the displacement from the ideal, defined as a percentage of the element-period i.e. the "percentage distortion" of that transition. Fig. 12C gives examples of "ideal", "early" and "late" transitions detected and also shows the action of the counter relative to the Up/Down Control, whilst Fig. 12D gives examples in greater detail, showing the relationship of the counter outputs for transitions distorted by specified amounts.

3.3.2 continued

IC's.4 and 6 are each 10-way b.c.d. up/down counters and form the "units" and "tens" stages respectively. IC.13(1-6) is MUP, the Up/Down Control which permits the counter to count up when pin 6 is high and down when pin 6 is low. MUP is set by the detection of "count 0-down" (CODOWN) at IC.21(4-6) causing pin 3 of IC.13 to go high, via IC.14 pin 3. It is reset by the detection of "count 49-up" (C49UP) at IC.21(1,2,13,12) causing pin 2 of IC.13 to go high via IC.21 pin 11. At these changeover points, the Up/Down Counter itself is prevented from stepping by a signal applied to the "count enable" input pin 13 of both IC.4-6, derived via IC.14(5,6;9,8 and 11,10), which is at 0v both at "count 0-down" and "count 49-up". This gives a "count 0" position either side of the "down-to-up" changeover point and a "count 49" position either side of the "up-to-down" changeover point as shown in Fig.12D. Gate IC's.28(8-11) and 12(4,5,6) are used to hold the counter in the "count 1-down" state when the Start/Stop Control is in its reset state (section 3.3.5) as shown in Fig.12D, whilst 27(11,10) and 14(13,12) are used to reset the counter to "count 0-up" for STOP PULSE measurement (see sections 3.3.5 and 3.3.8). IC.27(9,8) is used for "Phase-Locking" purposes (section 3.3.7).

3.3.3 Received Data Input Circuits (Fig.2A)

3.3.3.1 The signal input circuitry of the equipment consists of two amplifiers mounted on the mother board. The Waveform Display Amplifier converts the wide range of input levels to a signal capable of driving the Y scan circuit, whilst the Input Data Amplifier produces the 0v and +5v signal $\overline{\text{I/P DATA}}$ to drive the logic circuits. In order to produce a faithful representation of the input on the C.R.T., the former amplifier, comprising TR's 17 and 42, does not saturate and has a variable feedback as gain control called Waveform Amplitude, mounted on the rear panel.

An attenuation circuit precedes both amplifiers to reduce the high voltage input signals to a more manageable level. Signals from the front panel V24 terminal are attenuated by R's 22 and 23 in order that TR14 is working within its design limits over the full range of V24 specified levels. The attenuation network for the high level input is dependent on the mode of T.D.S.A. working i.e. series or shunt working as selected by the rear panel switch. For shunt working the input impedance is obviously required to be high, so the input from the front panel is attenuated by R24 and R22 before being converted to logic levels by the amplifier comprising TR's 9 to 14. In the series working mode the equipment is required to present a very small impedance to the line, so with switch 16 in the closed position, the line signals are detected across an 18 ohm resistor R21. Diodes D and D protect the input transistors against excessive voltage.

3.3.3.2 Threshold Detection

A further function performed at the input to the Input Data Amplifier is selection of the threshold voltage at which transitions are detected on a high level input signal. Provision is made for threshold detection on three types of high level input by selecting the required position on the front panel switch SW2.

3.3.3.2 continued

(a) Single Current +ve (SW2 position 3)

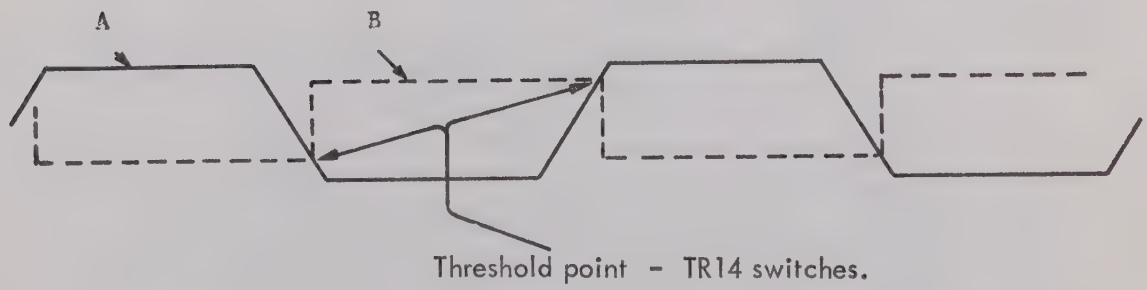
With the front panel input selector switch in this position, the threshold potentiometer, RV7, mounted on the rear panel, becomes part of a potential divider chain across the +15v rail through resistor R6 to R10. Threshold detection is made by comparing the potential on the wiper of RV7 with the input waveform at the common emitter pair TR14. When the voltage of a positive going transition on the R22 base of TR14 exceeds the threshold voltage on the other base, the potential at the junction of R20 and TR14 collector will fall to a level determined by the amount of constant current preset, by RV2. Negative going input transitions will cause TR14 to reset at the same threshold potential. TR14 collector waveform appears at the common emitter point of TR's 9 and 10, at the mean d.c. level of 0v, after a level change through zener diode D2. TR11 will reverse bias protection D1, is switched by this waveform to produce the logic level input to the digital circuitry $\overline{\text{DATA}}$.

(b) Single Current -ve (SW2 position 2)

For this type of input the threshold potentiometer RV4 is referenced to the -15v rail through R1.

(c) Double Current (SW2 position 1)

For this condition the output from the common emitters of TR's 9 and 10 is attenuated and fed back from RV4 wiper to TR14. The following waveform comparison is made by TR14.



Waveform A - Attenuated input waveform on TR14 base (R22).
Waveform B - TR14 base (Threshold potentiometer).

Diag.5.

As Waveform B is variable in amplitude, the point on the transition that TR14 changes state may be selected by the rear panel control. For correct threshold detection on double current the waveform at TR10 emitter must consist of equal voltage excursions about 0v. To obtain this condition the constant current through TR14 must be set by adjustment of RV2.

3.3.4 Input Data Retiming and Transition Detection (Fig.4)

The logic level input data signal $\overline{\text{I/P DATA}}$ (see section 3.3.3) is fed to a 3-stage shift register MT1, MTE and MT2. Here it is retimed to the 100 x element rate clock $\overline{\text{HSS}}$ and transition of input data detected by comparing the shift register stages with each other. During the "Down" or "Early" half-cycle of the Up/Down Counter this comparison is between the first two stages, $\overline{\text{MT1}}$ and MTE, a positive transition being detected if MT1 and $\overline{\text{MTE}}$ are both high and a negative transition of MT1 and MTE are both high. For the "Up" or "Late" half-cycle the comparison is between the second and third stages, MTE and MT2, where a positive transition is detected if $\overline{\text{MTE}}$ and MT2 are both high and a negative transition if MTE and $\overline{\text{MT2}}$ are both high. The "transition - detected" pulses so obtained are equal in width to one period of $\overline{\text{HSS}}$. The distortion display requires that the deflections produced for all distortion values other than 0% are only present for the first (or negative) part of $\overline{\text{HSS}}$, so that nominally the deflection is only for half the transition - detected pulse period. This is achieved by gating the transition - detected signals with a signal HSS', equivalent to HSS at all but the 0% time as decoded from the Up/Down Counter. HSS' is also gated with the "transition" signals from the "Hold Peak" Stores - see section 3.3.9.

$\overline{\text{I/P DATA}}$ is fed to MT1 set input on IC.27 pin 2 and the inverse to the reset input on IC.27 pin 3 via IC.26(13,12). Negative transitions are detected using IC.31(1,2,13,12; 11,10,9,8). During the "Early" half-cycle 31(11,10,9,8) is used, as pin 11 ($\overline{\text{MUP}}$) is high, whilst during the "Late" half-cycle 31(1,2,13,12) is used, as pin 1 (MUP) is high. The "wire OR'ed"combination of these two gates is fed to IC.14(9,8) to produce the "negative transition detected" signal NTD, a positive pulse, on pin 8. Similarly, positive transitions are detected using IC's.30(8-13) and 31(3-6). During the "Early" half-cycle (30(8-13)) is used as pin 9 ($\overline{\text{MUP}}$) is high, whilst during the "Late" half-cycle 31(3-6) is used as pin 3 (MUP) is high. The "wire OR'ed" combination of the two gates is fed to IC.29(1,2) to produce the "positive transition detected" pulse PTD on pin 2.

NTD and PTD gated with HSS' at IC's.21(4,5,6) and 21(1,2,3) respectively to produce $\overline{\text{TDN}}$ and $\overline{\text{TDP}}$. These latter signals are also controlled by the "Hold Peak" Distortion Stores "Transition Display" Modification Logic - see section 3.3.9. $\overline{\text{TDN}}$ is further taken through IC.7(13,12) to produce TDN which drives the appropriate input to the Y Summing Amplifier (section 3.3.11.4) to produce the Y deflections relevant to negative transition markers. $\overline{\text{TDP}}$ is taken through IC's.15(13,12,11) and 26(8,9) to produce $\overline{\text{TDP}}'$, which drives the Y Summary Amplifier input relevant to positive transition markers. The latter two gates are necessary to enable the insertion of the positive "blip" to mark the significant digits to the Error Counters (section); if the DISPLAY CONTROL switch SW6 is not set to ERROR STORE, $\overline{\text{DE}}$ on pin 15 of IC.15 is high, thus enabling $\overline{\text{TDP}}$ to switch $\overline{\text{TDP}}'$.

3.3.4 continued

HSS' is formed using IC.8(13,12,11;10,9,8). Pin 9 is controlled by HSS, whilst pins 13 and 12 are controlled by the Up/Down Counter count decode signals COT and COU, which go high during the "count 0-tens" and "count 0-units" periods respectively of the Up/Down Counter. IC's.13(10,9,8) and 7(10,11) are used to clamp HSS' to 0v when ERROR STORE is selected by the DISPLAY CONTROL switch SW6, when $\overline{DE}$ on pin 11 of IC.7 is taken to 0v. This is to prevent "distortion" transition markers being superimposed on the Error Count display.

IC.14(3,4;5,6) is used to produce $\overline{TDD}$, which is a negative-going pulse for each distortion marker to be displayed, used in the Blanking and "Bright-Up" Waveform Generation circuits (sections 3.3.14 and 15). $\overline{TDD}$ is also controlled from the "Hold Peak" Distortion Stores circuit and the Error Counters (to produce the positive "blip" previously mentioned). IC.14(11,10;13,12) is used to produce a similar signal to TDD, but which is not controlled by the "transition" signals from the "Hold Peak" Distortion Stores, for use in the Phase-Locking Circuit (section 3.3.7).

3.3.5 Start/Stop Control (Fig.5)

For START/STOP working as selected by SW7, Start/Stop Control consists essentially of a bistable, MS1, which is set when start polarity is detected on the data input and reset when the centre of the stop element of the incoming character is reached, or if a "short start" condition is detected in the Short Start Reject Circuit (section 3.3.6). If SW7 is set to FREE RUN or SYNC, however, another bistable, MS2 (Fig.3), will be set half an element period after MS1 which will inhibit any further reset to MS1.

MS1 (IC.18(1-6)) is set via its asynchronous input on pin 4, using IC. 19(1,2,13,12). The inputs on this gate are $\overline{MS1}$ on pin 1 and STPOL on pin 2, which goes high when start polarity is detected on the data input. STPOL is derived using IC's.19(3-6), 20(10,9,8) and 6(8-13), controlled by the START polarity switch SW3; $\overline{I/P\ DATA}$ on IC.20 pin 10 goes high when the actual data input to the instrument goes positive, whilst $\overline{PST}$ on pin 9 is taken to 0v when switch SW3 is set to "+". IC.19(1,2,13,12) is also used to set MGR - see section 3.3.8.

For START/STOP working, MS1 is reset when the middle of the stop element is reached. The stop element time is obtained by decoding the appropriate state of the Character-Length Counter in the "Character-Length Selection" gates and switching the result through IC.20(1,2,3) via pin 2, whilst the element centre time "count 49-up" is ANDed to the result by feeding $\overline{C49UP}$ through IC.20(4,5,6) via pin 5. The result is applied to the reset input of MS1, pin 2 of IC.18.

The signal $\overline{SHORT\ START\ REJECT}$ on pins 1 and 4 of IC.20 will go low if a "short start" is detected during the first 40% of the start element period (section 3.3.6), thus resetting MS1.

For FREE RUN and SYNC settings of SW7, bistable MS2 (IC.13(8-13) on Fig.3) will be set when the centre-point of the start element period has been

3.3.5 continued

reached, via IC.20(3,4;5,6). The inverse output of MS2 (IC.13 pin 8) is then used to clamp the reset input to MS1 (IC.18 pin 2 of Fig.5), so that MS1 remains set. To get out of this condition, switch SW7 would have to be returned to START/STOP; this will take $\overline{SS}$ on MS2 asynchronous reset input (IC.13 pin 10) to 0v, holding MS2 reset and therefore allowing MS1 to be reset.

3.3.6 Short Start Reject Circuit (Fig.3)

The Short Start Reject Circuit action can be selected by wire links on Board 1, such that the main Start Stop Control bistable MS1 will be reset if more than a preset amount of continuous stop polarity is detected during the first 40% of a supposed start element. A decade counter clocked by HSS, the 100 x element rate clock, is allowed to run if stop polarity is detected during this 40%, but is held reset when start polarity is present on the input data line. If the 10% S.S. REJ link is present, a reset will be applied to MS1 if the decade counter reaches its terminal count, thus indicating that a 10% period of continuous stop polarity has taken place. If the 5% S.S.REJ link is present, MS1 will be reset if the decade counter reaches a count of 5.

The decade counter is formed by the "9310" IC.5. The CEP (enable) and PE(preset) inputs are controlled by IC.7(5,6), which holds these points low when the Up/Down Counter count exceeds 40, and IC.28(1,2,13,12) via IC.7(11,10). Pin 13 of IC.28, controlled by IC.27(13,12), goes high when stop polarity is present on the input data line and the other two inputs on pins 1 and 2 of IC.28, MST4 and MST1 respectively (from the Character-Length Counter, section 3.3.8), define the first half of the start element. IC.28(4-6) is used to provide the reset to MS1 ($\overline{\text{SHORT START REJ}}$) for the 10% S.S.REJECT setting whilst IC.26(1-6) provides the reset for 5% S.S. REJECT.

3.3.7 Phase-Locking Circuit (Fig.4)

The purpose of the Phase-Locking Logic is to line up the zero point of the 50-way Up/Down Counter with the time when an "average" incoming data transition might be expected, i.e. to line up the "count 0" position with the "ideal transition" time. This is done by examing the relationship of these transitions to the Up/Down Counter count. If the transitions tend to occur more in the "early" or "down" half-cycle of count, then the length of count is reduced to 99 until the relationship is correct. On the other hand, if the transitions tend to occur more in the "late" or "up" half-cycle, then the length of count is increased to 101 until the correct relationship is achieved. The corrections are applied at the "count 0-down" time of the Up/Down Counter. When shortening the count, the Counter goes straight from the "count 0-down" to the "count 1-up" state, whilst when lengthening the count, it stays on the "count 0-down" position for two periods of HSS, the 100 x element-rate clock.

3.3.7 continued

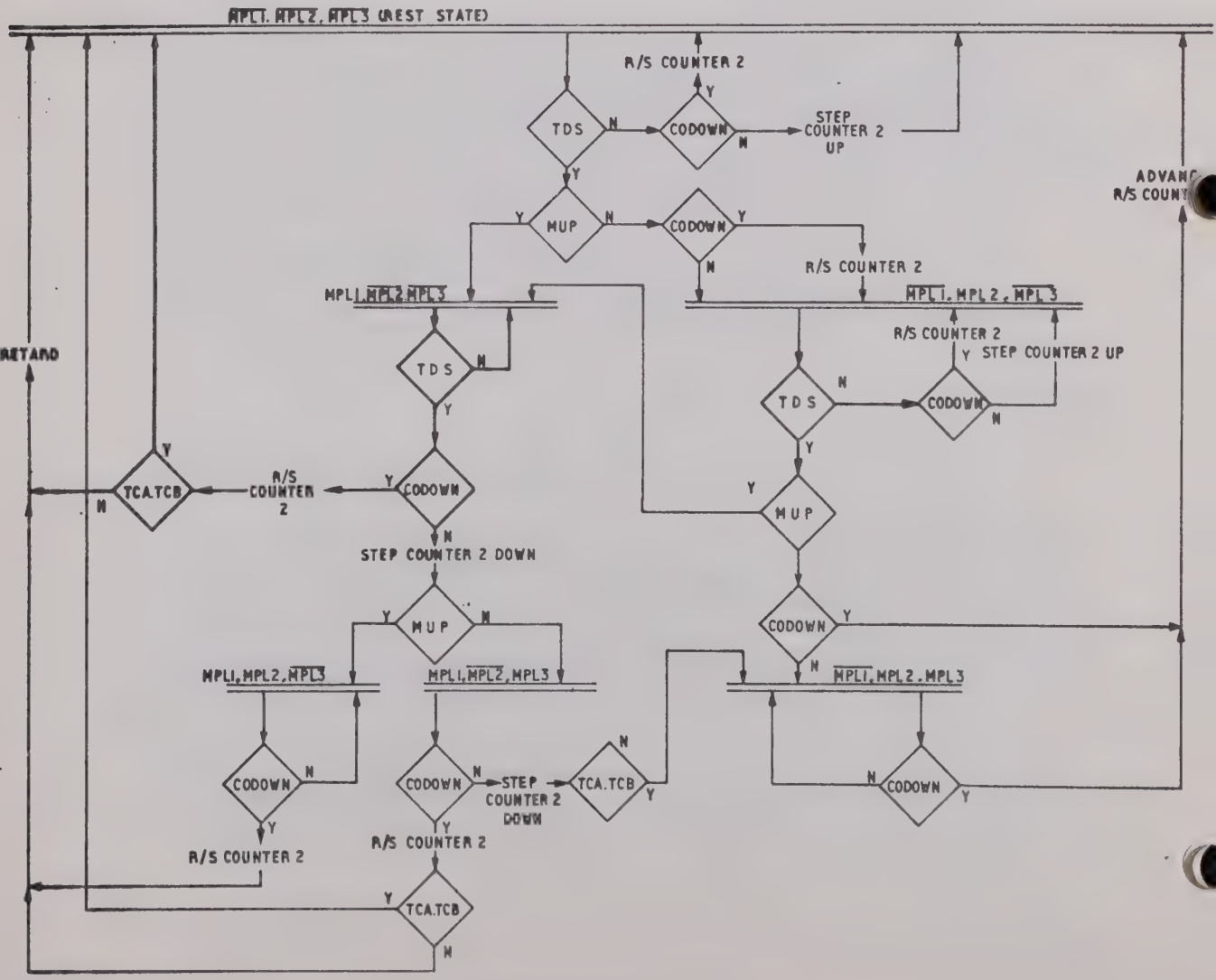
The type of correction to be applied is determined by comparing successive pairs of input data transitions as follows:

(a) If both transitions in a pair occur during the "early" or "up" half-cycle, then correction is applied to shorten (or "advance") the count;

(b) If both occur during the "late" half-cycle, then correction is applied to lengthen (or "retard") the count;

(c) If the two transitions occur during opposite half-cycles, then if the "early" transition occurs at a larger displacement from the counter zero point than does the "late" transition, "advance" correction is applied. Similarly, if the "late" transition is farther from the counter zero point than is the "early" transition, then "retard" correction is applied.

The phase-locking operation is controlled by a 3-stage counter, MPL 1-3, which is used to determine the sequence of actions. A subsidiary 50-way up/down counter is used for determining the relative displacement of successive "early" and "late" transitions. The action is best depicted using the following flow diagram, where the subsidiary up/down counter is referred to as "Counter 2":



FLOW DIAGRAM FOR PHASE-LOCKING ACTION
(SEE TEXT FOR TERMS USED)

AHB7697

DIAG. 6

3.3.7 continued

Note: (i) TDS is the "transition detected" signal from the Input Data Retiming and Transition Detection Circuit (section 3.3.4).

(ii) CODOWN defines the "count 0-down" period of the main 50-way Up/Down Counter.

(iii) TCA and TCB are the terminal count outputs of the first and second stages respectively of Counter 2, the subsidiary 50-way up/down counter.

(iv) MUP is the Up/Down Control bistable of the main 50-way Up/Down Counter. It is set (MUP high) during the "late" half-cycle and reset (MUP low) during the "early" half-cycle.

The 6 sets of double horizontal lines in the diagram represent the 6 combinations or "states" of MPL1-MPL3 which are used in the phase-locking sequence. The "diamond" symbols represent questions with "Yes" (Y) and "No" (N) answers. For example, starting from the "rest" state of $\overline{MPL1}.\overline{MPL2}.\overline{MPL3}$, if a transition is not present (TDS "N"), Counter 2 will be stepped in the up direction, except that if the main 50-way Up/Down Counter is on its "count 0-down" position (CODOWN "Y"), Counter 2 will be reset. If a transition is present (TDS "Y"), however, and the main Up/Down Counter is in its "up" half-cycle (MUP "Y"), then MPL1 will be set and the state of the Phase-Locking Circuit will now be $MPL1.\overline{MPL2}.\overline{MPL3}$. If the transition had occurred during the main Up/Down Counter's "down" half-cycle (MUP "N"), then MPL2 would be set instead and the state would become $\overline{MPL1}.MPL2.\overline{MPL3}$.

3.3.8 Character Length Counter (Fig.5)

This is a 4-stage binary counter, MST1-MST4, which for all positions of the DISPLAY CONTROL switch SW6 other than STOP PULSE is initially held in its "maximum count" position. When detection of start polarity on the data input causes the Start/Stop Control, MS1, to set (section 3.3.5) the counter is allowed to run, being stepped at the centre of each incoming data element period until the centre of the stop element period has been reached. At this point, and if the START STOP - FREE RUN - SYNC switch SW7 is set to START/STOP, MS1 will be reset and the C-L Counter Reset Control, MGR, set, which will reset the counter back to its "maximum count" position. This reset stays on until MGR itself is reset by MS1 being set again and the whole process repeated for the next character.

If the DISPLAY CONTROL switch is set to STOP PULSE the counter is still stepped at the centre of each element period, and when the centre of the step element period is reached and if SW7 is still set to START/STOP, MS1 will be reset, but the Character-Length Counter and Up/Down Counter (section 3.3.2) will be allowed to keep running until the next start polarity is detected on the data input. This sets MGR, which resets the Character-Length Counter to its "maximum count" position and the Up/Down Counter to "count 0-up" and sets MS1 (section 3.3.5). The process is then repeated for this next character.

3.3.8 continued

If SW7 is set to FREE RUN or SYNC, MS1 will not be reset again, thus allowing the counter to run continuously.

MST1-MST4 are formed by IC's. 12 and 13. The input clock to MST1 is MUP, the Up/Down Control on IC. 12 pin 1. MGR is IC. 18(8-13), pin 9 of which is the reset signal to the counter. The clocked set input to MGR for all but STOP PULSE measurement is derived via IC. 22(1,2;11,10;13,12); pin 11 is low as $\overline{\text{LOST}}$ on IC. 1 pin 11 is high (see Fig. 7A), $\overline{\text{C49UP}}$ on pin 1 is a signal from the Up/Down Counter which goes low at "count 49-up" and $\overline{\text{LAB}}$ on pin 13 is a signal which is low during the last state of the Character-Length Counter as selected by the ELEMENTS PER CHARACTER switch SW8 in the Start/Stop Control circuit. IC. 19(1,2,13,12) applies control via MGR's asynchronous input pin 10 on IC. 18; pin 1 is MS1's reset output and pin 2 is STPOL, a signal which goes high when start polarity as selected in the Start/Stop Control is present on the data input. The set output of MGR on pin 8 of IC. 18 is controlled by IC. 2(9,8); for other than STOP PULSE measurement, this output is clamped low by $\overline{\text{LOST}}$ on IC. 1 pin 9 being high, but for STOP PULSE measurement the signal LOST. MGR is used to set MS1 in the Start/Stop Control circuit (section 3.3.5) after start polarity has been detected.

3.3.9 "Hold Peak" Distortion Stores (Fig. 5)

These two stores are used to hold the maximum values of distortion for both "Early" and "Late" transitions of input data. When a transition is detected, the count of the 50-way Up/Down Counter at that instant is compared with the count held in one of the stores (the "Early" or "Late" store as appropriate). If the Up/Down Counter's count exceeds that held in the store, then the counter's count is fed into the store, together with the transition's polarity, to become the new "Hold Peak" value. The "Hold Peak" value of distortion is displayed by detecting when the Up/Down Counter and store counts agree and using this to insert a positive or negative "transition" marked as appropriate at that point. There is only one trace when the DISPLAY CONTROL switch SW6 is set to HOLD PEAK, even when SW7 is set to START/STOP; in this latter condition the 6-9 traces relevant to the SEP. ELEM DIST'N setting are combined into one (section 3.3.11) as the "Hold Peak" value of distortion is for all transitions.

The store for "Early" transitions consists of two 4-bit latches IC's. 3(1-11) and 4(13-23). IC. 4(10,11) is used to store the polarity of the transition, whilst the remaining 7 latches contain the BCD state of the Up/Down Counter which corresponds to the distortion of that transition. Similarly the "Late" Store consists of the two 4-bit latches IC's. 3(13,23) and 4(1-11), where IC. 4(10,11) stores the transition - polarity and the remaining latches store the BCD distortion of that transition.

The comparison of the Up/Down Counter and "Hold Peak" stores is done using the two "9324" comparator circuits, IC's. 16 and 17. The "A" set of inputs to the comparators is controlled by the "Early" Store outputs during the "Early" or "down" half-cycles of the Up/Down Counter and by the "Late" Store during the "Late" or "up" half-cycle. This is accomplished using IC's. 8,9,10(1,2,3;4,5,6;13,12,11) and 11(4,5,6;10,9,8;13,12,11) and signals MUP and $\overline{\text{MUP}}$ from the Up/Down Control bistable via IC. 2(11,10;9,8). The "B" set of inputs is controlled by the inverse outputs of the Up/Down

3.3.9 continued

Counter ($\overline{C1}$, $\overline{C2}$ etc.).

The Transition Polarity Selection gates are used to control whether the Store up-dates on positive only, negative only or all transitions. The signal NEG ONLY on IC.7 pin 9 can be taken to 0v by a back-panel link (Fig. 11) if storage of negative transitions only is required. Similarly, $\overline{\text{POS ONLY}}$ on IC.7 pin 12 can be linked to 0v if storage of positive transitions only is required. Signals NTD and PTD on IC.7 pins 10 and 13 are respectively the "negative transition detected" and "positive transition detected" pulses - see section 3.3.4. When a transition is detected and according to the POS ONLY/NEG ONLY linking, IC.7 pins 8 and 11 will go low, taking one "active low" Enable input of each 4-bit latch circuit low.

Up-dating of the "Early" store is controlled by IC.14(1,2,13,12). Pin 1 has a signal from the comparison circuit which is high when the Up/Down Counter's count is greater than the count in the store. Pin 2 is fed by a 100 x element rate signal which is formed by inverting $\overline{\text{HSS}}$ and applying a delay circuit so that the signal goes high approximately 300 nanoseconds after $\overline{\text{HSR}}$ has gone low; this is necessary to prevent the store being up-dated incorrectly at the Up/Down Counter switching times. Pin 13 has the "count down" signal $\overline{\text{MUP}}$ from the Up/Down Control bistable, which goes high for the "Early" half-cycle of the Up/Down Counter. Coincidence of all 3 signals plus a "transition detected" condition as determined by the Transition Polarity Selection gates will generate a "transfer" condition at the "Early" Store by taking both the "active low" Enable inputs of the 4-bit latches low, thus enabling the latches to take up the states of the Up/Down Counter outputs present on 7 of their "D" inputs. The remaining "D" input, IC.4 pin 22 is controlled by MT1 from the Input Data Retiming and Transition Detection circuit (section 3.3.4), so that the corresponding "Q" output on IC.4 pin 23 will go high if the transition which initiated the transfer action is positive.

Up-dating of the "Late" Store is controlled by IC.14(8-11). The signals on the inputs are the same as for the "Early" gate desdribed above, excepting that pin 9 has the "count up" signal MUP, which goes high for the "Late" half-cycle of the Up/Down Counter. In a similar manner to the "Early" Store up-dating, coincidence of all 3 signals plus a "transition - detected" condition causes the state of the Up/Down Counter to be staticised in the latch circuits, together with the transition polarity.

The stores are reset manually by operating the HOLD PEAK RESET push-button PB1, which takes signal $\overline{\text{DRS}}$ on the reset (MR) inputs of the latches to 0v.

The "Hold Peak" transition markers are inserted using IC's.7(1,2,3) and 15. IC.15(1-6) is used to modify the signal TDP, which provides the positive transition marker as described in section 3.3.4. Pin 1 is controlled by the "Early" Store "transition polarity" output (IC.4 pin 23) during the "Early" half-cycle; this is accomplished via IC's.10(10,9,8), 11(1,2,3) and 7(4,5,6). Pin 14 is controlled by the comparator circuit and goes high when the Up/Down Counter and Store counts agree. Pin 2 has the same "deflection modification" signal HSS' as is used for insertion of "actual transition" markers, described in

3.3.9 continued

section 3.3.4. Pin 5 is low unless HOLD PEAK is selected by SW6, when the signal $\overline{\text{HOLPK}}$ on IC.14 pin 5 will be at 0v.

IC.15(8-13) is used to modify the signal $\overline{\text{TDN}}$, which provides the negative transition marker as described in section 3.3.4. The inputs on IC.15 pins 13,10 and 12 are the same as those on pins 2,5 and 4 respectively (on the "$\overline{\text{TDP}}$" gate), whereas that on pin 9 is the inverse of that on pin 1 to insert markers of the opposite polarity.

IC.7(1,2,3) is used to modify $\overline{\text{TDD}}$ which gives the relevant control in the "Bright-Up" Waveform Generation circuit for insertion of transition markers (sections 3.3.13.1 and 3.3.15). Pin 2 is fed by the comparator signal which goes high when the Up/Down Counter and Store counts agree, whilst pin 1 is only high if $\overline{\text{HOLPK}}$ is at 0v on IC.14 pin 5.

3.3.10 C.R.T. X Deflection Circuit (Figs. 2A, 4 and 8)

The C.R.T. display in the X direction is made up of a series of dots corresponding to logic level information from the digital circuitry. This type of read-out has the advantage of being accurate without the need for complicated alignment against cursor lines.

3.3.10.1 Pump Circuit (Fig.2A)

Conversion from digital to analogue signals for the timebase is made using the Pump Circuit (Fig.2A). The signal input to the Motherboard from the logic is called PUMP, and takes the form of a square wave containing as many positive edges as there are dots required across the C.R.T. screen. This waveform is amplified by TR39 to present a 30v square wave to the pump input capacitor, C5. TR38, the pump transistor, is a common base amplifier with a predominantly capacitive load, C6. The negative edges of the waveform on C5 cause TR38 to conduct and so increase the negative charge across C6. As the collector of TR38 is a very high impedance point, C6 retains its charge until the next negative edge on C5, thereby producing a negative going staircase waveform. For normal start stop working the staircase consists of 99 steps, which is reset at a command from the logic by discharging C6 with TR36. The pump is reset by a positive pulse on the pump reset input REPUMP which turns off TR33, allowing TR3 to conduct due to the base current through R99. An impedance buffer, formed by emitter follower TR34 and 35, is used to couple the timebase waveform from TR38 collector to the input of the X Scan Amplifier mounted on the sub-board (Fig.8). As the X sensitivity of the C.R.T. varies from tube to tube the timebase waveform amplitude is preset by adjusting the A.O.T. capacitor C7.

When using the instrument as an input waveform monitor, the display requirement changes from one element per scan to one character per scan. As the number of dots required for one element is 100, the timebase waveform when displaying a character contains the following number of steps:-

$$100 \times (\text{No. of Elements/Character} + 1.5)$$

3.3.10.1 continued

The reason for the additional 1.5 is that the whole of the start pulse and half a bit of stop pulse are included in the character display. To maintain the timebase waveform amplitude for correct scan length, with a greater number of steps, the pump input waveform on C5 is reduced in amplitude. This reduction is made by switching on TR41 for 5 bit input characters, and TR40 for 6,7 and 8 bit input characters.

3.3.10.2 Pump Input Waveform Generation (Fig.4)

The Pump Circuit input signal PUMP is for the most part equivalent to HSS, the 100 x element-rate clock. When displaying distortion, the effect of the cycle of HSS that occurs during the "count 0-up" period of the Up/Down Counter is gated out, so that the calibration dot positions on the C.R.T. screen for "count 0-down" and "count 0-up" are superimposed; put another way, this is so that the 0% Early and 0% Late marker positions are the same on the screen. When displaying start/stop distortion or the state of the Error Counters, the pump signal is also inhibited during the "all 1's" state of the Character-Length Counter.

PUMP is formed at IC.19(8-11). Pin 9 contains the 100 x element-rate signal $\overline{HSS}$. Pin 10 has the signal which inhibits PUMP at the "count 0-up" position whilst pin 11 has the signal which inhibits PUMP during the "all 1's" state of the C-L Counter.

3.3.10.3 Pump Reset Generation

The Pump Circuit is reset by the signal REPUMP formed on bistable MFB IC.28(1-6). For the distortion and Error Count display, this bistable is set by the "count 49-up" signal from the Up/Down Counter, i.e. at the end of each scan of marker dots, for all scans, except the last one, when displaying start/stop distortion or the state of the Error Counters. For the latter two conditions, MFB is set just before the beginning of the first trace. Once set, MFB is always reset half a period of HSS later via its asynchronous input. For the INPUT WAVEFORM position of SW6, MFB is set half an element-period after the beginning of the stop pulse, i.e. at the end of the last state of the Character-Length Counter.

The "end of trace" signal $\overline{C49UP}$ is applied to MFB's set input via IC.26(11,10). The remaining control to this point is applied via IC.26(5,6), ans is as follows:

> IC.21(13,12,11) is used to enable the input for all scans except the last. LAB on pin 12 goes low during the last scan, i.e. the last state of the Character-Length Counter, whilst $\overline{DIC}$ on pin 13 is high for all positions of SW6 other than INPUT WAVEFORM. IC.26(3,4), on the other hand, is used to enable the input during the last state of the C-L Counter (LAB) for the INPUT WAVEFORM, STOP PULSE and non start/stop DISTORTION settings of SW6, as detected by IC.6(1,2,13,12).

MFB is reset using IC.21(10,9,8), which has $\overline{HSS}$ on pin 9 and $\overline{MUP}$ (from the Up/Down Control) on pin 10; the effect of this is to apply a negative pulse on IC.28 pin 4 half a period of HSS after the beginning of each trace.

3.3.10.4 X Scan Amplifier (Fig.8)

The X Scan Amplifier, comprising TR's 6 to 10 mounted on the sub-board is a differential type using the input on TR7 base for the scan waveform, and the TR10 base input for X shift. Both input transistors are high frequency amplifiers driving the high voltage common base transistors, TR6 and 9. Quiescent current in both legs of the amplifier is set to approximately 5mA by the constant current transistor TR8. Diodes D3 and 4 are protection against an excessive negative voltage at the input and resistors R19 and 27 are included to prevent either input transistor being switched off, which would limit the speed of operation.

Front panel controls include a horizontal magnifier which increases the gain of the amplifier by connecting the 680 ohm resistor R21 across R22 and R23. This gives an increase in gain of approximately 2.5 times on all switch positions except X1. High frequency gain compensation is provided in the form of C6 and C7 to speed up flyback on the magnified and X1 gain positions respectively. Adjustment of these A.O.T. capacitors is made by connecting a high impedance, low capacity oscilloscope probe to each X output point (TR's 6 and 9 collector). With the probes feeding into a dual trace oscilloscope, the latter being set to add algebraically one normal and one inverted trace, the capacitors are adjusted on their respective gain ranges for optimum flyback conditions at 9.6 Kbits/sec, i.e. not slow and rounded caused by too little capacity and no overshoot caused by too much capacity. Fig.12A gives typical examples of waveforms. The final A.O.T. capacitor, C3, compensates for the removal of the oscilloscope probes and is adjusted for overall picture improvement at 9.6 Kbits/sec by observing the C.R.T. display.

3.3.10.5 Switched X Shift Adjustment (Fig.8)

On position 3 and 4 of the Horizontal Magnifier switch (50%E to 10%E and 10%L to 50%L), the required X shift is internally generated by the sub-board circuitry comprising TR's 11 to 15. Position 3 of the switch connects the logic signal $\overline{EE}$ (Expand Early) to 0v. This signal is routed via R92 on the motherboard to the emitter of TR12 on the sub-board and causes the latter transistor to conduct. A collector current of 1mA, set by R92 4.7K, pulls down the base, and hence emitter of TR11 to a voltage determined by R32 and R33 in parallel. TR11 then increases the current through the lower leg of the X shift potentiometer chains, taking the base of TR10 positive, which centres the early part of the X scan on the C.R.T. Because of a tolerance on the C.R.T. X sensitivity, the amount of X shift required is preset for a given tube by the A.O.T. resistor R32. To generate the required X shift on switch position 4, the logic signal $\overline{EL}$ (Expand Late) is routed through R93 on the motherboard to TR14 on the sub-board. The circuit action is similar to that previously described, but with one more inversion, such that TR15 increases the current through the upper leg of the X shift potentiometer chain, pulling TR10 base more negative. Once again the amount of X shift is preset by the A.O.T. resistor R39.

3.3.11 C.R.T. Y Deflection Circuit (Figs.2A, 4 and 8)

Four types of waveform are required for Y deflection:-

3.3.11 continued

(i) A step waveform for the SEP. ELEM DISTN (START/STOP only) STOP PULSE and ERROR STORE (type 1A only) positions of the DISPLAY CONTROL SWITCH, to give the appropriate number of "element transition" scans.

(ii) A steady "mid-screen" condition for the HOLD PEAK DISTN and SEP. ELEM DISTN (FREE RUN and SYNC modes), where a single scan of marker dots is required.

(iii) Positive and negative transition markers for all but the INPUT WAVEFORM display.

(iv) The input data waveform when set to INPUT WAVEFORM.

The step waveform of (i) is derived using the Digital to Analogue Converter Circuit (Fig. 2A) to convert the states of the binary Character Length Counter into discrete voltage steps on the input to the Y Summing Amplifier. The transition markers of (iii) are also added in at this point to give the basic Y deflection waveforms SUM. AMP, which is amplified by the Y Summing Amplifier and then fed via the DISPLAY CONTROL switch SW6 (Fig. 10) (in all but the INPUT WAVEFORM position) to the final Y Scan Amplifier (Fig. 8) which drives the Y plates. The "mid-screen" position of (ii) is obtained by holding the D to A Converter inputs to a fixed condition.

For the INPUT WAVEFORM display of (iv) the output of the Waveform Display Amplifier, WAVEFORM (Fig. 2A), is fed via SW6 to the Y Scan Amplifier.

3.3.11.1 Digital to Analogue Converter (Fig. 2A)

The type of D to A converter used to generate the Y step waveform is of a binary input form, and consists of the circuitry TR's 27 to 33. A four section converter is used because when displaying the two bit stop pulse of an eight bit character, eleven traces are required. The input condition for the top trace of an elements separated display is all 1's from the logic, i.e. DA's 1 to 4 all positive, forcing TR's 28, 30, 31 and 32 into a bottomed condition. The D to A output from the emitter follower TR29 is then 0v, rising in steps of approximately 0.9v with each updated binary input, to a possible maximum of 15 steps. In order to maintain a constant impedance in the switched resistor chains to either +14v or 0v, dependant upon the transistor state, the diodes D6, 10, 11 and 13 short circuit one of the 10K resistors in the transistor off condition.

When working in the elements separated condition the minimum number of steps required is dive and the maximum eight, but for a single trace display the logic provides the correct polarity inputs to the D to A for a mid-position d.c. level out. To display a useful Y amplitude in a five or eight elements per character separated display, the switched Y gain transistor TR23 is controlled from the front panel switch by logic functions $\overline{5BCH}$ and $\overline{DE}$ (T.D.S.A. Type 1A). For a six, seven or eight element display the cathodes of D4 and D5 are at +5v, allowing R37 to hold TR23 in the bottomed condition short circuiting R36.

3.3.11.1 continued

This resistor forms part of the potential divider chain R's 36,38 and 39 on the output of the D to A converter, and its value is chosen such that with TR23 on, a 9 trace display fills the screen and with TR23, a 6 trace display fills the screen. For the TR23 off condition, 0v is applied to either $\overline{5BCH}$ or $\overline{DE}$, the latter control being to provide a 6 trace error measurement display for the T.D.S.A. Type 1A.

3.3.11.2 Digital to Analogue Converter Input Generation (Fig.4)

To give the step waveform described in section (i), the logic controlling the D to A Converter inputs arranges that for the STOP PULSE position of SW6, DA1 is equivalent to the output $\overline{MST1}$ of the 1st bistable stage of the Character-Length Counter, DA2 equivalent to $\overline{MST2}$ from the 2nd bistable, DA3 to $\overline{MST3}$ from the 3rd bistable and DA4 to $\overline{MST4}$ from the 4th bistable. The same is true for the SEP.ELEM DIST (START/STOP only) and ERROR STORE positions of SW6, except that the "DA" signals are switched to give the "middle scan" position when the Character-Length Counter is in the "all 1's" condition, i.e. for the period starting one-half of a unit element after the beginning of the stop element and ending at the mid-point of the next start element;stated alternatively, this is the period between the end of the last scan for one character and the beginning of the first scan for the following character.

For the condition described in section (ii), the logic arranges the "DA" inputs to give the "middle scan" position continuously. When the ELEMENTS PER CHARACTER switch SW8 is set for 5-unit characters, the middle scan is considered to be the 4th one, i.e. the scan for displaying the transition time between the 3rd and 4th information elements. For 6-8 unit characters the 6th scan position is selected.

The "DA" inputs are formed using IC's.12,20(1,2;3,4;5,6;11,10;13,12) and 13(1,2,3). Selection of the middle scan is done using IC's.6(3-6) and 7(1,2). IC.6 pin 5 is taken low when HOLD PEAK is selected by SW6. Pin 4 always remains high. Pin 3 is controlled by IC.13(4,5,6;13,12,11); it will be held low.

(a) if SYNC or FREE RUN is selected by SW7 and SW6 is not set to ERROR STORE, in which case the signals $\overline{DE}$ and $\overline{SS}$ on IC.13 pins 5 and 4 respectively will be high.

or (b) if the Character-Length Counter is in its "all 1's" state, as detected by signals MST3 and MST4 on IC.13 pins 12 and 13 respectively being high.

When the middle scan is selected, IC.6 pin 6 goes high, and IC.7 pin 2 low, thus preventing the Character-Length Counter outputs ($\overline{MST1}$, $\overline{MST2}$ etc.) from switching the "DA" signals.

3.3.11.3 Y Summing Amplifier

IC.5, a linear integrated circuit type LM301, is used to add positive and negative transition markers to the D to A waveform. It is operated as an inverting amplifier, the two functions being fed in via input resistors R40 and R41 to pin 2. Transition markers are derived in the logic as $\overline{TDP}$ (negative pulses coinciding with positive transitions) and TDN (positive pulses coinciding with negative transitions). Variable gain, controlled by RV4 in the feedback loop, is used to compensate for the C.R.T. Y sensitivity tolerance, and covers a range of about 0.8:1 to 1.2:1. The 150pF capacitor C10 connected between pins 1 and 2 of IC.5, acts as a speed-up capacitor, by-passing the p.n.p. stage within the IC. and thus improving the device slew rate. Frequency compensation in the form of C15, and supply de-coupling capacitors C14 and 16 are the remaining discrete components required to operate the amplifier.

3.3.11.4 Y Scan Amplifier

This amplifier, mounted on the sub-board is similar to the X scan amplifier (section 3.3.10.4) but has no facility for changing the gain. Internally generated Y shift is applied in one direction by the circuitry comprising TR's 16,17 and 18, which is operated when measuring stop pulse length by the front panel logic signal $\overline{LOST}$.

3.3.12 E.H.T. Box (Fig.9)

This unit consists of two circuit boards and a transformer mounted in a copper plated plastic box, the whole being secured to the rear panel by four nylon screws. TR1, the oscillator transistor, is also mounted on the rear panel for heat dissipation purposes. A simple feedback oscillator is used to convert a 30v stabilised input to the required C.R.T. supplies. The transformer, wound on two Mullard ferrite E cores type FX 1106, has a 12 turn primary winding and a 2 turn feedback winding, C2 being selected for an operating frequency of approximately 25 KHz. Oscillation amplitude is adjusted by means of R1, the A.O.T. resistor, and is initially set to give a potential of -490v at pin 6. Four transformer secondary windings provide the C.R.T. supplies as follows:

Sec 1 - Output 1375 peak into voltage quadrupler D's 3,4,5 and 6 for a C.R.T. final anode supply of +5500v.

Sec 2 - Output 490v peak half wave rectified by D1 for -490v C.R.T. cathode supply.

Sec 3 - Output 550v peak half wave rectified by D2 for -550v brightness control potentiometer.

Sec 4 - Output 11v r.m.s. for C.R.T. heaters.

C.R.T. Brightness is controlled by varying the potential on grid 1 from the brightness pot connected between -490v (cathode) and -550v, this allowing -60v for cut-off. The front panel focus control completes a potential divider chain with R's 4 and 5 to supply a focus electrode voltage range of 100v to 220v with respect to the cathode. All supplies to and from the E.H.T. box

3.3.12 continued

are connected to the rest of the unit by plug 12 which mates with a socket mounted on the motherboard.

3.3.13 C.R.T. Control Circuits

D.C. conditions for the C.R.T. are arranged such that the majority of the electrodes with signals on are referenced to mean potentials of approximately 100v, therefore capable of being directly driven by transistor circuitry. For this reason the cathode is operated at -500v and the final anode at +5500v, giving a p.d.a. potential of 6KV.

3.3.13.1 "Bright-up" and Blanking Circuits (Figs. 2A and B)

Brightness modulation is used to produce C.R.T. trace markers in the form of bright-up for 10% and blank for 0% indication. Bright-up pulses are formed in the logic and routed to the motherboard (Fig.2A) as BRIGHT, these are amplified and inverted by TR26 and a.c. coupled to grid 1 of the C.R.T. As there is a tolerance on the grid cathode potential for a given display brightness, the amplitude of the bright-up pulses is set for a particular tube by adjustment of the A.O.T. resistor R74. The signal BRIGHT is also generated when a transition is detected, being used to bright-up the transition markers when the display is set to Distortion Display. In addition to this, the logic signal TDD is used by TR21 on the sub-board (Fig.8) to increase the size of the bright-up pulse applied to grid 1 of the C.R.T.

Grid 2 is a separate electrode provided in the C.R.T. for blanking, and is driven by the sub-board circuit (Fig.8) comprising TR's 19 and 20 which converts the logic input BLANK to large amplitude negative pulses referenced to a potential of approximately +110v. Because the circuit is required to blank 1% marker dots at high bit rates, a high speed switching transistor TR20 is used to control a high voltage transistor TR19 with a relatively low output impedance.

3.3.13.2 Astigmatism (Fig.2A)

This control, mounted on the front panel, forms part of a potential divider chain with R66 on the motherboard, to supply a voltage range of 125v to the C.R.T. electrode o3.

3.3.13.3 Trace Curvature (Fig.2A)

This effect is reduced to a minimum by adjustment of the screen control preset potentiometer, RV3, mounted on the underside of the motherboard.

3.3.13.4 Twist Control (Fig.2A)

Twist compensation for the square faced tube is made by adjustment of RV6 mounted on the motherboard. This preset control is used to vary in both directions the current through a twist coil, which is positioned around the neck of the C.R.T.

3.3.14 Blanking Waveform Generation (Logic, Fig. 4)

The signal BLANK on IC.15 pin 8 goes high whenever "blanking" of the C.R.T. trace is required.

This occurs on:

(i) the 0% marker position for the HOLD PEAK DISTN, SEP.ELEM DISTN and STOP PULSE positions of SW6, unless a transition marker is being displayed;

(ii) the period starting one-half of a unit element after the beginning of the stop element and ending one-half of a unit element after the beginning of the next start element, when SW6 is set to HOLD PEAK DISTN or SEP.ELEM DISTN and SW7 to START/STOP;

(iii) the period starting after the start element transition has been detected and ending at the centre of the last information element, when SW6 is set to STOP PULSE;

(iv) the period starting one-half of a unit element after the beginning of the stop element and ending at the beginning of the next start element when SW6 is set to INPUT WAVEFORM and SW7 to START/STOP;

(v) the periods outside the displayed trace(s) for the X3 positions of the HORIZONTAL MAGNIFIER when SW6 is set to HOLD PEAK DISTN or SEP.ELEM DISTN;

(vi) the periods between the marker dots for the ERROR STORE position of SW6.

BLANK is formed on IC.15(10,9,8). To meet the requirements of (ii) and (iv), pin 10 has a signal common to the Pump Input Waveform Generation circuit (section 3.3.10.2), which goes low during the "all 1's" state of the Character-Length Counter when SW7 is set to START/STOP and SW6 to any position other than INPUT WAVEFORM; it will also go low during this period if SW6 is set to ERROR STORE, regardless of the setting of SW7. If SW6 is set to INPUT WAVEFORM, then the signal will also go low if MS1, the Start/Stop Control bistable, is reset.

IC.15(4,5,6) is used to insert the blanking signals of (i), (iii) and (v), by controlling IC.15 pin 9. Pin 4 contains the signal DD, high for all but the INPUT WAVEFORM and ERROR STORE positions of SW6. IC.6(8-11) is used to insert the 0% blanking of (i) via IC.8 pin 4, whilst IC.8 pin 5 is controlled by IC.25 (to insert the blanking described in (iii)) and IC's. 29(3,4;5,6) and 22(1,2,3;4,5,6) (to insert the blanking described in (v)).

The blanking described in (vi) is effected by controlling the signal $\overline{\text{BLANKE}}$ on IC.15 pin 10 from Logic Board 5 (Fig.7); this is described in section 3.3.21.

3.3.15 "Bright-Up" Waveform Generation (Logic, Fig.4)

The signal $\overline{\text{BRIGHT}}$ is used to "bright-up" the 10% and transition markers for the distortion displays. The logic to accomplish this is on Logic Board 2 (Fig.4). "Bright-up" markers are also produced at intervals of 10% of a signal element when INPUT WAVEFORM is selected and the HORIZONTAL MAGNIFIER switch SW5 is set to one of the "X3" positions; the logic to accomplish this is on the Mother Board (Fig.2B). The signal $\overline{\text{BRIGHT}}$ is "active low", hence its "NOT" designation.

On Fig.4, IC.18(8-13) is used to insert the distortion display 10% and transition markers. Pin 9 has a signal common to the Pump Input Waveform Generation circuit (section 3.3.10.2), which goes low during the "all 1's" state of the Character-Length Counter when SW7 is set to START/STOP and the DISPLAY CONTROL switch SW6 to any position other than INPUT WAVEFORM; it will also go low during this period if SW6 is set to ERROR STORE, regardless of the setting of SW7. Pin 12 contains the signal DD ("Distortion Display"), formed on Logic Board 3 (IC.21(1-6) on Fig.5), which goes high if SW6 is set to HOLD PEAK DISTN, SEP.ELEM DISTN or STOP PULSE. Pin 13 contains a signal which goes low when blanking is required for the "X3" positions of the HORIZONTAL MAGNIFIER, or for the start and information element period when set to STOP PULSE - see section 3.3.14. Pin 10 has a signal which goes high when a 10% marker dot or a transition marker is to be displayed; TDD on IC.15 pin 1 is the negative going transition marker pulse described in section 3.3.4, whilst the 10% marker control is exercised using IC.8(1,2,3).

The INPUT WAVEFORM 10% "bright-ups" are accomplished using IC.1 on the Mother Board (Fig.2B). If any of the "X3" positions are selected by the HORIZONTAL MAGNIFIER switch SW5, then one of signals $\overline{\text{EM}}$, $\overline{\text{EL}}$ or $\overline{\text{EE}}$ on pins 4, 3 or 5 respectively will be taken to 0v. If SW6 is set to INPUT WAVEFORM then $\overline{\text{DIC}}$ on pin 1 will also be at 0v, thus raising pin 11. The remaining signal on pin 9 is COU, formed on Logic Board 2 (Fig.4), which goes high when the "units" stage of the Up/Down Counter is on count 0, thus the signal BRIGHT on IC.1 pin 1 will be taken low at 10% intervals.

3.3.16 Fox and Q9S Message Error Detection (Fig.6)

Errors in an incoming FOX or Q9S message are detected by comparing it with a locally derived message. The latter message is obtained by addressing the Read-Only Memory (ROM) with the Message-Length Counter. The ROM presents the characters of the message in parallel form to the Local Start/Stop Character Generation circuit, where they are serialised and retimed on bistable MRD. The output of MRD is compared with the incoming message in the Start/Stop Character Error Detection Circuit, where bistable MCE becomes set for each character in error, being reset at the end of each character. The incoming message has to be delayed for two periods of $\overline{\text{HSS}}$ through the Input Data Delay Register, MDD1 and MDD2, to compensate for timing differences between the incoming and locally generated data.

3.3.16 continued

The Element Sampling Point Generation circuit (section 3.3.19) is used to generate the strobe used for sampling the comparison between the two data streams; this strobe can be switched in 5% steps from the 5% Early and Late points of the element to the 45% Early and Late points, using the ERROR THRESHOLD switch SW14 on the rear panel of the unit.

The Start/Stop Message Phasing Control circuit (described below) holds the Message Length Counter initially in the reset state, corresponding to the first character position of the message being received, e.g. "Line Feed" in the case of either FOX message. When the incoming character agrees with this locally-generated character, the reset to the M.-L. Counter is removed and the counter is allowed to step at the end of each character, thus keeping the locally-generated message in phase with the incoming message.

The Start/Stop Message Phasing Control consists of a decade counter which is reset at the end of each error-free character, but which is incremented each time a character-error is detected. If 9 consecutive characters are found to be in error, an "out-of-phase" condition is considered to exist, denoted by the "terminal count" (ETC) on IC.25 pin 15 of the decade counter being present. It is this latter condition wh used to hold the M.-L. Counter in its reset state.

3.3.16.1 Message-Length Counter (Fig.6)

This is a six-stage binary counter, the purpose of which is to define the character positions in the FOX or Q9S messages. The M.-L. Counter Reset Control bistable MRL is used to reset the counter to zero when the end of the message is reached. For the two FOX messages, the 2 x LF, CR Control bistable MDLF is used to make the counter cycle through its first two states twice because of the double line feed, carriage return sequence at the beginning of each message. Additional resets are applied to the counter when phasing.

The counter itself is formed by bistables ML1-ML6. ML1 changes state with each "end-of-character" signal present on pins 2 and 3 of IC.5, whilst the rest of the counter is "ripple-through". The "end-of-character" signal is formed using IC's.11(4,5,6) and 9(1,2). For the FOX messages, the 2 x LF, CR control MDLF controls the input to ML2 via IC.11(13,12,11), so that ML2 will set until ML1, which clocks MDLF on IC.4 pin 13, has set and reset once.

For the Q9S message, however, Q9S on IC.11 pin 13 will be low, thus holding pin 11 high and allowing the counter to count without interruption. When running normally, the M.L. Counter Reset Control bistable MRL is set when the end of the sequence is detected, using IC's. 19(3,4;5,6), 11(1,2,3;10,9,8) and 16(1,2,13,12), thus resetting the counter by taking the asynchronous inputs of ML2-ML6 and MDLF low, it is unnecessary to reset ML1 at this point as the bistable resets itself.

When the Start/Stop Phasing Control is in its "out-of-phase" condition, signal $\overline{\text{ETC}}$ on the asynchronous inputs of MRL and ML1 will be low, thus holding the M.-L. Counter reset. $\overline{\text{ETC}}$ is also taken low via IC.22(3,4)

3.3.16.1 continued

and TR2 when the PHASE push-button PB2 is pressed, when PHASE on IC.22 pin 3 will go low.

3.3.16.2 Read-Only Memory and Local Start/Stop Character Generation (Fig.6)

The information elements of the FOX and Q9S message characters are stored in the ROM which is addressed by the M.-L. Counter (previous section). Each character is produced at the ROM output in the form of 5-8 parallel bits of information. These are serialised in the local Start/Stop Character Generation circuit, where "start" and "stop" elements are also added, before being fed to the Start/Stop Character Error Detection circuit (next section).

IC's.6 and 7 are DM8810's, the high-level drivers required to drive the ROM address inputs A1-A6. The ROM outputs B1-B8 are fed to IC.20, a "9312" eight-input multiplexer circuit, which is used to serialise the data under the control of the Character-Length Counter outputs MST1', MST2' and MST3'. IC's.3 and 2 (13,12;1,2;5,6) are used to determine the required polarity of start and information elements for the local data, as selected by the START and INFO.EL switches SW3 and SW4 on the front panel. The resultant serial signal is sampled at the '0%' point of the Up/Down Counter, the '0%' signal being formed at IC.18(8-13) and applied via IC.2(9,8;11,10). It is then retimed at bistable MRD.

3.3.16.3 Start/Stop Character Error Detection and Start/Stop Message Phasing Control (Fig.6)

IC.1(4,5,6;10,9,8) is used to compare the incoming message with the locally-generated message. The result is strobed by a signal from the Element Sampling Point Generation circuit (section 3.3.19) via IC.22(1,2;13,12) and the result used to set bistable MCE when an error is detected. MCE is reset at the end of each character by the same signal that is used to step the M.-L. Counter.

The reset output of MCE is fed to the clock input IC.25 pin 2 of the "9310" decade counter of the Start/Stop Message Phasing Control, so that the counter will be stepped at the end of each character in error. At the end of each error-free character, however, a reset will be applied to the counter via IC.26(3-6). When 9 consecutive characters are in error, the counter will reach "count 9" and the terminal count output ETC on IC.25 pin 15 will go high, forcing pin 7 low via IC.19(1,2) and thus maintaining the counter in this position until an error-free character is detected again. Whilst signal ETC is present, the M.-L. Counter is held reset. This condition is also used to control the IN PHASE lamp via IC.23(10,9,8) on Board 5 (Fig.7), which drives IC.9(3,4) and TR1 on Board 4 (Fig.6) which in turn drive the lamp.

3.3.17 Parity Error Detection (Fig.6)

This circuit consists of a bistable MPAR which is reset at the beginning of each character and then allowed to switch every time an information element that is a "1" is detected on the retimed incoming data (bistable MR1 on Fig.7). For the E PARITY position of ERROR COUNT CONTROL switch SW12, an error will be recorded if MPAR and MR1 disagree at the end of a character, whilst in the O PARITY position an error will be recorded if MPAR and MR1 agree at this time. MR1 is the first stage of the register used in the Pseudo-Random Generation.

IC.23(1-6) is used to reset MPAR at the beginning of each character; MST1, MST2 etc. are outputs from the Character-Length Counter. IC.16(8-11) is used to sample MR1 (Pin 10) at the element centre C49UP(M) (Pin 11) and set and reset MPAR via IC's. 9(9,8) and 15(10,9,8). Odd or Even parity error detection is determined using IC.15(1,2,3;13,12,11); $\overline{POD}$ on pin 1 goes low when SW12 is set for Odd parity whilst $\overline{PEV}$ on pin 13 goes low for Even parity. IC's.1(13,12,11), 11(9,10) and 15(4,5,6) are used to compare MPAR and MR1. The result is sampled by the same "end-of-character" signal that drives the Message-Length Counter at IC.26(1,2,13,12); pin 2 contains the "end-of-character" signal, pin 13 the result of MPAR and MR1's comparison and pin 1 $\overline{HSS}$, the 100 x element-rate clock. The latter condition is included to gate our transition spikes.

3.3.18 Pseudo-Random Sequence Error Detection (Figs. 6 & 7)

Errors in an incoming 511-bit pseudo-random data stream are detected by comparing it with a locally-generated data stream. The latter sequence is derived using the Pseudo-Random Generator (Fig.6) which is aligned with the incoming data by means of the P-R Phasing Control. Errors are detected by comparing the first stage of the register in the P-R Generator with the output of the Input Data Delay Register (Fig.6) and strobing this either with the output of the Element Sampling Point Generation circuit (Fig.6, section 3.3.19), or CENTRE, the "P-R Centre-Sampling Strobe for Error Check" formed on Board 5 (Fig.7). The Input Data Delay Register is used to delay the incoming data by two periods of $\overline{HSS}$, to compensate for timing differences between the incoming and locally-generated data.

3.3.18.1 Pseudo-Random Generator and Phasing Control (Fig.7)

The P-R Generator is a 9-stage shift register, where the outputs of the fifth and ninth stages are combined in an "Exclusive OR" gate and the result fed back to the first stage. The "all 1's" state of the register is used to set bistable MPRS to derive the P-R Block Timing pulse. The register is clocked by an element-rate signal derived under the control of the P.-R. Phasing Control circuit, as described later. For phasing, this clock consists of a narrow pulse occurring at the element mid-point, so that the received data signal which is being clocked into the register is sampled at the optimum point. When phasing is complete, the clock reverts to being a square wave, the positive edge occurring at the same time position as the narrow pulse would have done but the negative edge now occurring 50% of an element later; as the register switches on negative clock-edges, this means that data derived from the register will have the same nominal bit-phase as the incoming data.

3.3.18.1 continued

The P-R Phasing Control also controls the input to the 2nd stage MR2 of the register. When phasing, this input consists of the "normalised input data" signal DATAN, whilst when phasing is complete the input is taken from the first stage MR1, so that the 511-bit pattern is circulated. DATAN is formed under the control of the INFO.EL polarity switch SW4, such that a Mark on the INPUT terminal will result in DATAN going positive, regardless of the actual polarity at the terminal.

The P-R Phasing Control circuit consists of two bistables, MPR1 and MPR2, which control the inputs, reset and clock line to the P.-R. Generator. When both bistables are reset, the register-clock consists of a square wave, the negative edges of which coincide with the nominal transition-times of the incoming data . Depressing the PHASE button will take the signal $\overline{\text{PHASE}}$ on MPR1's asynchronous input low and thus set the bistable. This in turn will cause MPR2 to be set on the next clock pulse, but before this happens the condition MPR1.$\overline{\text{MPR2}}$ is used to clear the register. When MPR2 has set, the clock to the register becomes the element mid-point narrow pulse described earlier, in order to clock data into the register via MR2's inputs. When data has been clocked right the way through the register, detected by MR9 becoming set, MPR1 is reset and in turn this resets MPR2, thus reverting the register clock back to the square wave and MR2's inputs to being supplied by MR1.

DATAN and $\overline{\text{DATAN}}$ are derived using IC's.27(10,9,8;13,12,11) and 29(1,2). The input to MR2 is swit ched using IC.35(10,9,8;13,12,11;1,2,3). The "Exclusive OR" gate on MR1's input is formed by IC.19(1,2,3;4,5,6) and the result applied via IC.27(1,2,3). For P-R working, pin 2 of IC.27 is high but for all other settings of the ERROR COUNT CONTROL SW12 this signal is low and MR1 is fed by DATAN (via IC.27(4,5,6), principally so that in either of the PARITY positions of SW12, MR1 can supply a retimed incoming data signal for parity error detection (see section 3.3.17). The "all 1's" signal is detected on IC.3(8-13).

For the P-R Phasing Control, the register-reset signal is applied using IC. 19(13,12,11). The mid-point sampling pulse is made up using IC.12(8-13), R19, C1 and IC.11(10,9,8) in a straightforward pulse-shortening circuit. The input to this circuit is derived from either the Up/Down Control bistable MUP or the external element-rate ELEMENT TIM. I/P. The latter signal is selected by the USE EXT.EL.TIMING link being present in the Tag Board on the Rear Panel (Fig.11A), when signal $\overline{\text{EXEL}}$ on IC.20 pin 9 is taken to 0v. The selection between the narrow and square wave clock signal for the register is done using IC's.11(4,5,6) and 12(1-6), the latter also providing the drive requirement. IC.29(3,4;5,6;9,8) is used to provide the centre-sampling strobe required for error checks (next section).

If the P-R AUTO REPHASE link is present, phasing will be initiated at the end of every block which contains one or more errors, using IC.28(1,2,13,12) to control the signal $\overline{\text{PHASE}}$. Pin 1 is controlled by MPR5, the P-R Block Timing bistable, pin 2 by the Block Error signal obtained from IC.21 pin 8 (see next section), whilst pin 13 will only be high if the ERROR COUNT CONTROL SW12 is set to either of the 511 P-R positions.

3.3.18.2 Element and Block Error Detection (Fig.6)

Elements in error in the P-R sequence are detected by comparing MR1, the first stage of the P-R Generator register, with MDD2, the output of the Input Data Delay Register. This comparison is strobed either with the output of the Element Sampling Point Generation circuit (section 3.3.19) or by the mid-point strobe signal CENTRE if either the USE EXT.EL.TIMING link is present on the rear panel tag board or the ERROR THRESHOLD % switch SW14 is set to 50. This comparison is used to set bistable MRE, which will reset itself one period of $\overline{HSS}$ later. The Block Error Detection circuit consists of a pair of "gate" IC's cross-coupled to form a bistable. This bistable is switched one way whenever the "element-error" bistable MRE is set and is switched back the other way at the end of the 511-bit block as detected by MPRS, the P-R Block Timing bistable.

MR1 and MDD11 are compared using IC.21(4,5,6;10,9,8). IC.18(1-6) is used to strobe this comparison with the output of the Element Sampling Point generation; pin 1 contains HSS to prevent unwanted switching spikes whilst pin 5 is low when centre-sampling is required, as described in the previous paragraph. The "50%" setting of SW14 is detected using IC.22(5,6;9,8;11,10). Centre-sampling of the data-comparison is done using IC.16(3-6).

The Block Error Detection "cross-coupled" bistable is formed by IC.17(3,4) and, on Board 5 (Fig.7), IC.21(10,9,8). IC.23(8-11), R29, C1 and IC.1(1,2,3) (all on Fig.6) are used to shorten the signal $\overline{MPRS}$ from the P-R Block Timing bistable, to give a narrow reset pulse to the Block Error bistable.

3.3.19 Element Sampling Point Generation (Fig.6)

The function of this circuit is to generate a strobe one period of HSS wide to sample the comparison of incoming data with locally-generated data for the purpose of error detection. This strobe is used in both Pseudo-Random Sequence Error Detection (section 3.3.18.2) and Fox and Q9S Message Error Detection (section 3.3.16.3).

The circuit consists of a "9324" comparator circuit whose A=B output goes high when the Up/Down Counter is on the clock times selected by the ERROR THRESHOLD % switch SW14 on the back panel (Fig.11A). The inverse ouputs of the 10's stage of the Up/Down Counter are fed to the first 3 "B" inputs of the comparator whilst the switch outputs, which are "inverse BCD" except for $\overline{SEL5}$ are fed to the "A" inputs. $\overline{COUNT\ 5}$ is applied to the "B3" input to give the intermediate "5%" strobe points whilst COU is applied to the "B4" input to give the "10%" strobe points.

3.3.20 Error Counters (Fig.7)

There are two 3-decade counters, which can be used either to count different functions in parallel or to count the same function in series where Error Counter No.2 acts as an extension to Error Counter No.1; this action is controlled by the COUNTER 2 function switch SW15 on the rear panel.

3.3.20 continued

The functions to be counted are selected via the Error Counter Input Gating. When the counters have reached a count of 999 or a total series count of 999,999 (depending on whether the OVERFLOW function has been selected or not), an inhibit is applied to prevent further counting. Inhibits are also applied when phasing to any of the standard Start/Stop messages on the 511-bit P-R sequence.

For Error Counter No.1, IC.21(13,12,11) is used to enable character errors to be counted for the 5U FOX CHAR, 8U FOX CHAR and Q9S CHAR positions of the ERROR COUNT CONTROL switch SW12. IC.30(1,2,13,12) enables element errors to be counted for the 511-P-R ELEM position of SW12 whilst IC.28(3-6) enables block errors to be counted in the 511 P-R BLOCK position. IC.11(13,12,11) is used to apply an inhibit to the first counter decade when the counter is full. IC36(5,6) applies an inhibit during phasing to Start/Stop messages and IC's.35(4,5,6) and 11(1,2,3) applies an inhibit during phasing to P-R sequences.

For Error Counter No.2, IC.30(3-6) enables the counter to act as an overflow to Error Counter No.1 in the OVERFLOW position of SW15 on the rear panel. The number of P-R Blocks or Start/Stop Messages received is counted using IC.31(9,8) in conjunction with IC's.31(11,10) and 13(13,12,11;10,9,8). The number of Automatic Rephasing actions when receiving start/stop messages is counted using IC.14(1,2,13,12) and Block Errors are counted using IC.14(3-6). IC.31(5,6) applies an inhibit to the first counter decade when the counter is full. IC.36(1,2;3,4) applies an inhibit during phasing to P-R sequences.

3.3.21 Error Display Control (Fig.7)

The error count display is a modified form of the normal "Element Separated" distortion display for a 5-unit character. The tube display consists of 6 horizontal lines of up to 10 dots, where each line represents the decode of a particular counter decade and the number of dots in the line represents the count (0-9) in that decade. These lines of dots are basically the distortion display traces where all but the "5%" marker dots have been blanked out. For each line, the dot representing the "significant digit" of the associated counter decade is given a deflection similar to that for a positive transition in the distortion display, whilst the rest of the line is held blanked out.

The "significant digit" dot is detected by comparing the state of the error counter decade with the state of the "Marker" Counter. This latter counter is also a decade counter, which is reset at the end of each trace scan and stepped for each possible digit position, i.e. at the points corresponding to the 5% markers of the distortion display.

To compare this counter with each of the Error Counters in turn, the "Marker" Counter outputs are fed to the Equivalence Detection circuit "B" inputs, whilst Multiplexer circuits are used under the control of the Character-Length Counter to select the four "A" inputs to the Equivalence Detection circuit; each Multiplexer is fed by the same stage of each decade, so that one Multiplexer selects the "1's" input to the comparator, the next the "2's", the

3.3.21 continued

next the "4's" and the last the "8's". The A=B output from the Equivalence Detection circuit is used to give the "positive transition" marker and also to set bistable MBL. This bistable remains set until the end of the trace scan and whilst set causes the display to be blanked. The Blanking Control also arranges that the intervals between the error display markers are blanked.

IC's. 17, 18, 25 and 26 are the "9312" Multiplexer circuits used to select respectively the "1's", "2's", "4's" and "8's" inputs to the "9324" comparator IC. 16, the Equivalence Detection circuit, which compares these inputs with those obtained from the "Marker" Counter IC. 24. Signal $\overline{\text{COUNT 5}}$ on the ENABLE input on IC. 16 pin 1 goes low at the "5%" points referred to earlier, so that the Equivalence Detection circuit can only give an output at these times. The same signal is used to step the "Marker" Counter. This counter is reset at the end of each scan by the signal C49UP(M), applied via IC. 22(9,8) to its present input on IC. 24 pin 9.

3.3.22 Power Supplies (Figs. 2A and 11)

Mains input to the unit is routed through a 1 amp anti-surge fuse and switch to a mains voltage selector mounted on the rear panel. The front panel mains indicator is connected across the 240v transformer primary to make it independant of input voltage.

3.3.22.1 D.C. Supplies (Fig. 11)

The following d.c. supplies are derived from four transformer secondaries, rectified by diodes mounted on the transformer tag panel, and stabilised, with the exception of the +250v, on the mother board.

(a) +250v. Bridge rectified by diode D1 to D4 and smoothed by C1 and R1. This rail is not stabilised and is used for tube controls and scan amplifiers.

(b) +30v. Bridge rectified by diodes D5 to D8 and smoothed by C2. This rail when stabilised on the mother board is used for E.H.T. and X timebase generation.

(c) +15v and -15v. Half-wave rectified from a common transformer winding by diodes D9 and D10 and smoothed by C's 3 and 4. These supplies, after stabilisation, are used widely for the conversion from digital to analogue signals.

(d) +5v. Full-wave rectified by diodes D11 and D12 mounted on the rear panel for heat sink purposes and smoothed by C's 5 and 6. This supply is stabilised and used mainly for driving the digital integrated circuits.

3.3.22.2 Supply Stabilisers (Fig. 2A)

All four stabilisers, mounted on the mother board, are of a conventional design using a differential amplifier, the output of which drives the final series transistor via an emitter follower. Therefore the following description of the

3.3.22.2 continued

+15v stabiliser applies in principle to the remaining three. The non-inverting input of the differential amplifier, TR1 base, is held at a constant voltage by the 5.6 zener diode D9, while the inverting input, TR2 base, is used to sense variations on the stabiliser output. A positive variation on the +15v line will cause a corresponding negative variation at TR2 collector, and as there is no inversion through TR3 and TR4 the output will return to its set level. RV1 is a preset voltage control primarily to set the +15v output, but as all stabilisers use the +15v line for a reference, this control affects all stabilised outputs. Adjusting RV1 to set the +5v ensures that all stabilised supplies are within the design limits. The differential amplifier in the +5v stabiliser is an integrated circuit type 741, which gives the advantage of high gain with low offset voltage.

CHAPTER 4

MAINTENANCE INSTRUCTIONS

4.1 Access to the Instrument

WARNING: Isolate the T.D.S.A. from the mains supply before dismantling.

4.1.1 Access to the plug-in sub-boards may be gained by removing the top cover after unscrewing four 3mm Pozidrive screws located at each corner of the cover.

N.B. Care should be taken when removing the following sub-board. (See General Assembly.)

Board 1 - Disconnect the coaxial connection from the front panel.

4.1.2 For removal of the front panel it is necessary to take off the carrying handle, top cover and bottom cover, the latter being held in place by four 3mm screws located at the feet centres. The carrying handle may be disconnected by unscrewing the studs on the side panels using a 4mm hexagon socket wrench. Four 3mm countersunk screws securing the front panel are then accessible, located two each side of the unit. Before complete removal of the front panel the following connections should be removed:

a) PL 11 - Mounted on the left hand side panel and used to connect the mains input to the front panel ON/OFF switch.

b) PL 10 - Mounted on the left hand side panel and used to connect d.c. supplies to the mother board stabilisers.

c) Coaxial connection to board 1 used for variable oscillator frequency control.

The front panel may then be carefully removed from the mother board 100-way edge connector.

4.1.3 Front panel knobs may be removed by pulling out the plastic centre piece which exposes either a hexagon headed or screwdriver slotted collet nut. Loosening the nut by half to three-quarters of a turn will allow the knob to be withdrawn.

4.1.4 Replacement of faulty front panel components will in the case of the following controls require removal of the decorative plate:

All lever switches
Brilliance Control
Focus Control
Astigmatism Control
±20% Variable Speed Control
$\bar{x}$ and y Shift Control

4.1.4 continued

The decorative plate is secured in place by all the components not listed above. The light emitting diodes are mounted in plastic clips and may be pressed out from the front of the panel. The mains ON indicator is a neon, held in position by a nut at the rear of the panel.

4.1.5 For access to the C.R.T. the front panel must first be removed as described in 4.1.2. Slacken the two screws on the C.R.T. front support bracket, which clamp the mu-metal screen, partly remove the tube and remove the base connection, E.H.T. connection, and twist coil flying leads at the mother board. The C.R.T. complete with its mu-metal screen may then be withdrawn from the equipment.

4.1.6 In order to adjust certain C.R.T. display parameters it is necessary to operate the equipment with the mother board mechanically remote from the left hand side extrusions. To separate these sub-units, the front panel and right hand side panel must first be removed. The latter has no wiring or components attached to it so may be disconnected from the rear panel after removing four 3mm countersunk screws. After removing the mother board rear support, a 3mm screw located on its underside, and the two printed circuit board plugs PL's 6 and 7 the board may be moved clear of the left hand side panel components. To restore the equipment to an electrically operational condition, the front panel must be connected to the mother board 100-way edge connector with PL 10 and PL11 re-connected.

4.1.7 Rear panel components include power transistors, 5v rectifying diodes and E.H.T. box. Access to these components may be gained by removing top and bottom covers, all plug-in boards, plugs PL 6, PL 7 and PL 12, eight 3mm screws, four on each side, and the mother board rear support screw. The rear panel may then be laid flat in an accessible position. If the E.H.T. box is removed from the rear panel it must be replaced using nylon screws.

4.2 Replacement of Components on Printed Circuit Boards

4.2.1 All printed circuit boards in this equipment, with track on both sides, have plated through holes. It is, therefore, only necessary to solder components on the underside of each board. When changing components on these boards the use of a hot soldering iron together with a solder sucking tool is recommended.

4.3 Adjustment of Preset Controls

4.3.1 Stabilised Supplies

All stabilised supplies are referenced to the +15v rail, and may be set up by adjusting RV1, on the underside of the mother board, for the correct potential on the +5v line to be 5.1v $\pm$200mV.

4.3.2 ±20% Variable Oscillator

This oscillator should be adjusted such that its frequency when set to NOM is equal to that of the fixed oscillator. To achieve this connect an input to the unit that produces a 0% transition marker on the bottom trace of an element separated display when switched to a fixed speed. Set the variable speed control to NOM and switch to the UNCAL position. Adjust C7 on board 1 for a display corresponding to that on the fixed oscillator, i.e. a 0% transition marker on the final trace.

4.3.3 x Scan Amplitude

To allow for the C.R.T. manufacturer's tolerance on x plate sensitivity, C7 is adjusted for the correct trace length on each particular tube. An increase in the value of C7 reduces the trace length.

4.3.4 x Amplifier High Frequency Compensation

High frequency compensation for this amplifier is provided by A.O.T. capacitors C6 and C7, the values of which may be selected in the following way:

a) Set up two 10:1 probes using the square wave output from an oscilloscope with a dual trace facility.

b) Connect these probes, one to each of the two x plate outputs on the sub-board, and earth both locally to 0v.

c) Set the oscilloscope to add one normal and one inverted channel of the same gain.

d) Set the T.D.S.A. for a X1 elements separated display on FREE RUN at 9600 BITS/SEC.

e) Adjust C7 on the sub-board for an oscilloscope waveform as close as possible to the ideal waveform shown in Fig. 12A.

f) Switch EXPANDED TRACE to X3 30%E and adjust C6 for the condition given in (e).

g) Remove both oscilloscope probes and set EXPANDED TRACE to X1.

h) Adjust C3 for the optimum spacing of displayed dots in the x direction between 40% and 49% early.

4.3.5 x Shift Preset

Adjustment for the amount of preset x shift required, when increasing the gain of the x amplifier by the EXPANDED TRACE switch, is made by A.O.T. resistors R32 and R39 in the sub-board. The former resistor should be adjusted to centralise the trace on X3 30%E and the latter on X3 30%L.

4.3.6 y Gain Preset

A small amount of adjustment on the display y amplitude is provided by RV4 on the underside of the mother board.

4.3.7 y Amplifier High Frequency Compensation

High frequency compensation for this amplifier is provided by the A.O.T. capacitors C3 and C12, the values for which may be selected in the following way:

a) Set up two 10:1 oscilloscope probes as in 4.3.4(a) and connect them to the y plate outputs on the sub-board.

b) Connect to the input of the T.D.S.A. a 5 unit continuous signal with all 5 elements in a negative condition, and set the controls to view this on an elements separated display at 9600 bits/sec.

c) Using the oscilloscope delayed trace facility, expand the transition marker on the first flat portion of the staircase waveform.

d) Adjust C3 on the sub-board for an oscilloscope display as close as possible to the ideal waveform shown in Fig. 12B.

e) Remove both oscilloscope probes and adjust C12 to compensate for any overshoot, on the transition or flyback points, due to the probe removal.

4.3.8 Twist Correction

Compensation for any display twist on the square faced C.R.T. is provided by RV6, on the underside of the mother board.

4.3.9 Trace Curvature Correction

Adjustment of RV3 on the underside of the mother board will provide trace curvature correction, and should be set in conjunction with the front panel ASTIG control.

4.3.10 10% Markers

A.O.T. resistor R74 provides adjustment for the amplitude of brightness modulation on the 10% markers.

4.3.11 Threshold Detection Preset

After replacement of certain input amplifier components, RV2 on the underside of the mother board may need resetting in the following way:

a) Connect to 1:1 V24 waveform to the input of the T.D.S.A.

b) Set the instrument for shunt working and monitor the junction of TR9 and TR10 emitters with an oscilloscope.

c) Adjust RV2 until the oscilloscope waveform has equal amplitude positive and negative transitions.

ORDERING PROCEDURE

All parts listed in this Section may be obtained from Trend Communications Limited. Prices will be quoted on application. The following information should be given in any enquiry or order for spare parts:

(a) The instrument Type Number

(b) The instrument Serial Number, if known.

(c) The Trend Part Number for Trend parts

(d) The Circuit Reference and Assembly Part Number for non-Trend parts. The component type and value is also required.

(e) If an Assembly Part Number or Circuit Reference is not applicable or not known, a full description of component type, maker and type number should be given.

(f) In the case of Mains operated components, the supply voltage and frequency should be given.

USE OF ALTERNATIVES

The components listed in the following sections are those normally fitted at the time of preparation of this handbook. However, Trend Communications Limited pursue a policy of competitive purchasing, and different components and different suppliers may be used from time to time.

The most important characteristics of the passive components used are listed, and in most cases many compatible alternatives are available. These equivalents may be fitted if the listed components is not available, but if any doubt exists as to the suitability of any component, Trend Communications Ltd. should be consulted. In the case of semi-conductor components, so many parameters have to be taken into consideration that it is not possible to list the characteristics required of an alternative. Generally, the listed components should be used exclusively, and if not readily obtainable from the usual stockists they may be obtained from Trend Communications Ltd.

5.1 COMPONENT LIST - MOTHER BOARD ASSEMBLY

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R1	6K8	±5%	.5w	Carbon Film
R2	4K7	"	"	"
R3	4K7	"	"	"
R4	15K	"	"	"
R5	15K	"	"	"
R6	6K8	"	"	"
R7	100	"	"	"
R8	100	"	"	"
R9	A.O.T.			
R10	2K2	"	"	"
R11	3K9	"	"	"
R12	680	"	"	"
R13	1K	"	"	"
R14	1K	"	"	"
R15	4K7	"	"	"
R16	2K2	"	"	"
R17	1K8	"	"	"
R18	4K7	"	"	"
R19	10K	"	"	"
R20	4K7	"	"	"
R21	18	"	"	"
R22	2K2	"	"	"
R23	6K8	"	"	"
R24	100K	"	"	"
R25	10K	"	"	"
R26	4K7	"	"	"
R27	8K2	"	"	"
R28	15K	"	"	"
R29	1K	"	"	"
R30	8K2	"	"	"
R31	27K	"	"	"
R32	27K	"	"	"
R33	1K5	"	"	"
R34	4K7	"	"	"
R35	1K	"	"	"
R36	1K	"	"	"
R37	1K	"	"	"
R38	180	"	"	"
R39	150	"	"	"
R40	2K7	"	"	"
R41	2K7	"	"	"
R42	2K2	"	"	"
R43	1K8	"	"	"
R44	10K	"	"	"
R45	10K	"	"	"
R46	20K	"	"	"
R47	10K	"	"	"
R48	10K	"	"	"
R49	15K	"	"	"
R50	1K	"	"	"

5.1 COMPONENT LIST - MOTHER BOARD ASSEMBLY continued

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R51	4K7	±5%	.5w	Carbon Film
R52	1K8	"	"	"
R53	10K	"	"	"
R54	2K2	"	"	"
R55	4K7	"	"	"
R56	1K	"	"	"
R57	4K7	"	"	"
R58	6K8	"	"	"
R59	4K7	"	"	"
R60	6K8	"	"	"
R61	4K7	"	"	"
R62	10K	"	"	"
R63	10K	"	"	"
R64	1K	"	"	"
R65	Not used			
R66	39K	"	"	"
R67	47K	"	"	"
R68	5K6	"	"	"
R69	47K	"	"	"
R70	68K	"	"	"
R71	Not used			
R72	Not used			
R73	Not used			
R74	A.O.T.			
R75	680	"	"	"
R76	10K	"	"	"
R77	10K	"	"	"
R78	Not used			
R79	10K	"	"	"
R80	10K	"	"	"
R81	1K8	"	"	"
R82	10K	"	"	"
R83	10K	"	"	"
R84	10K	"	"	"
R85	10K	"	"	"
R86	1K8	"	"	"
R87	10K	"	"	"
R88	10K	"	"	"
R89	10K	"	"	"
R90	10K	"	"	"
R91	1K8	"	"	"
R92	4K7	"	"	"
R93	4K7	"	"	"
R94	1K5	"	"	"
R95	10K	"	"	"
R96	4K7	"	"	"
R97	2K2	"	"	"
R98	680	"	"	"
R99	1K5	"	"	"
R100	Not used			

5.1 COMPONENT LIST - MOTHER BOARD ASSEMBLY continued

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R101	Not used			
R102	Not used			
R103	56K	±5%	.5w	Carbon Film
R104	1K	"	"	"
R105	2K2	"	"	"
R106	130	"	"	"
R107	1K	"	"	"
R108	2K2	"	"	"
R109	180	"	"	"
R110	1K	"	"	"
R111	1K	"	"	"
R112	47	"	"	"
R113	2M2	"	"	"
R114	22K	"	"	"
R115	100	"	"	"
R116	1K8	"	"	"

Circuit Ref.	Value μ Farads	Maximum Tolerance	Minimum Working Voltage	Maker and Description
CAPACITORS				
C1	A.O.T.	±20%	20v	
C2	68	±20%	40v	Erie 20102 Electrolytic
C3	68	±20%	40v	" "
C4	68	±20%	40v	" "
C5	47p	±10%	50v	Erie HI-K Type YD
C6	0.033	±10%	20v	Wima Tropyfol M
C7	A.O.T.			
C8	100	±20%	10v	ITT 26176 Electrolytic
C9	220p	±20%	20v	Erie HI-K Style AD
C10	150p	±20%	10v	Erie HI-K Style YD
C11	22p	±20%	10v	" "
C12	0.022	±20%	40v	Mullard C281
C13	0.01	±20%	500v	Erie HI-K Style 811
C14	1.5	±20%	20v	Tag
C15	10p	±20%	10v	Erie 10DN
C16	1.5	±20%	20v	Tag
C17	0.22	±20%	80v	Mullard C281 - VV
C18	0.01	±20%	40v	Erie Transcap
C19	0.01	±20%	40v	"
C20	0.01	±20%	40v	"
C21	0.01	±20%	500v	Erie HI-K Type 811
C22	0.01	±20%	500v	" "
C23	0.022	±20%	40v	Erie Style AD

5.1 COMPONENT LIST - MOTHER BOARD ASSEMBLY continued

Circuit Ref.	Type
TRANSISTORS	
TR1	BC107
TR2	BC107
TR3	BC107
TR4	BFY51
TR5	BFX87
TR6	BCY70
TR7	BCY70
TR8	BCY70
TR9	BCY70
TR10	BC107
TR11	BSX19
TR12	BC107
TR13	BC107
TR14	2N2910
TR15	Not used
TR16	BFY51
TR17	2N2910 or BFY82
TR18	Not used
TR19	BC107
TR20	BC107
TR21	BC107
TR22	BFY51
TR23	BSX19
TR24	BC107
TR25	Not used
TR26	BSX19
TR27	Not used
TR28	BSX19
TR29	BC107
TR30	BSX19
TR31	BSX19
TR32	BSX19
TR33	BSY41
TR34	BC109 or 2N2484
TR35	BC107
TR36	BFX87
TR37	Not used
TR38	BSX19
TR39	BSX19
TR40	BC107
TR41	BC107
TR42	BC107

5.1 COMPONENT LIST - MOTHER BOARD ASSEMBLY continued

Circuit Ref.	Type
DIODES	
D1	IN4148
D2	BZY 88C10
D3	IN4148
D4	IN4148
D5	IN4148
D6	IN4148
D7	Not used
D8	Not used
D9	BZY 88 C5V6
D10	IN4148
D11	IN4148
D12	IN4148
D13	IN4148
D14	BZY 88C 3V3
D15	IN4148
INTEGRATED CIRCUITS	
IC1	D962
IC2	D936
IC3	D936
IC4	uA741
IC5	LM301

Circuit Ref.	Value ohms	Type	Maker
RESISTORS VARIABLE			
RV1	1K	567-00HS	Daystrom
RV2	500	"	"
RV3	50K	"	"
RV4	1K	"	"
RV5	Not used		
RV6	2K	"	"

Circuit Ref.	Description and Maker
MISCELLANEOUS	
SKT1	Ferranti Edge Connector EWD 32/32FS
SKT2	" "
SKT3	" EWD 40/40FS
SKT4	" " (Not used on Type 2A)
SKT5	" " (" ")
SKT6	McMurdo Edge Connector Single sided MP1485 (16-way)
SKT7	" " " (")

5.2 COMPONENT LIST - LOGIC BOARD 1

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R1	1M	±5%	.5w	Carbon Film
R2	470	"	"	"
R3	5K6	"	"	"
R4	1K	"	"	"
R5	6K8	"	"	"
R6	5K6	"	"	"
R7	510	"	"	"
R8	2K2	"	"	"
R9	220	"	"	"
R10	2K2	"	"	"
R11	2K2	"	"	"
R12	3K3	"	"	"
R13	1K	"	"	"
R14	1K	"	"	"
R15	1K	"	"	"
R16	1K	"	"	"
R17	Unallocated			
R18	1K	"	"	"
R19	1K	"	"	"
R20	1K	"	"	"
R21	1K	"	"	"
R22	1K	"	"	"
R23	1K	"	"	"
R24	1K	"	"	"
R25	1K	"	"	"
R26	1K	"	"	"
R27	1K	"	"	"
R28	1K	"	"	"
R29	1K	"	"	"
R30	18K	"	"	"
R31	3K3	"	"	"
R32	1K	"	"	"
R33	1K	"	"	"
R34	1K	"	"	"
R35	1K	"	"	"
R36	1K	"	"	"
R37	1K	"	"	"
R38	1K	"	"	"
R39	1K	"	"	"
R40	1K	"	"	"
R41	1K	"	"	"
R42	1K	"	"	"
R43	10K	"	"	"
R44	100K	"	"	"
R45	5K6	"	"	"
R46	100	"	"	"
R47	100	"	"	"
R48	100	"	"	"
R49	330	"	"	"

5.2 COMPONENTS LIST - LOGIC BOARD 1 continued

Circuit Ref.	Value u Farads	Maximum Tolerance	Minimum Working Voltage	Maker and Description
CAPACITORS				
C1	0.01	±20%	20v	Wima Tropyfol F
C2	47p	±10%	20v	Wima Tropyfol F
C3	1000p	±10%	20v	Wima Tropyfol F
C4	47p	±10%	20v	Wima Tropyfol F
C5	0.01	±20%	20v	Wima Tropyfol F
C6	150p	±10%	20v	Erie
C7	5p - 25p	-	20v	Erie Trimmer 557c
C8	0.01	±20%	20v	Wima Tropyfol F
C9	150p	±20%	20v	Wima Tropyfol F
C10	100p	±20%	20v	Wima Tropyfol F
C11	330p	±20%	20v	Wima Tropyfol F

Circuit Ref.	Type
TRANSISTORS	
TR1	BCY70
TR2	BSX19
TR3	BSX19
TR4	BC107
TR5	BSX19
TR6	BC107
TR7	BSY41
TR8	BSX19
TR9	BSX19
TR10	BCY70
TR11	BC107
DIODES	
D1	IN4148
D2	IN4148
D3	IN4148
D4	IN4148
D5	IN4148
D6	IN4148
INTEGRATED CIRCUITS	
IC1	D9093
IC2	D9093
IC3	D9093
IC4	D9306
IC5	D9310
IC6	D9306
IC7	D936
IC8	D9093
IC9	D9093
IC10	D9093
IC11	D9093

5.2 COMPONENT LIST - LOGIC BOARD 1 continued

Circuit Ref.	Type
INTEGRATED CIRCUITS	
IC12	D946
IC13	D9093
IC14	D936
IC15	D936
IC16	D946
IC17	D936
IC18	D930
IC19	D946
IC20	D936
IC21	D962
IC22	D946
IC23	D946
IC24	D962
IC25	D962
IC26	D962
IC27	D936
IC28	D962
IC29	D932
IC30	D936

Circuit Ref.	Description and Maker
MISCELLANEOUS	
X1	2.88 MHz Crystal Type MMW - Cathodeon

5.3 COMPONENT LIST - LOGIC BOARD 2

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R1	1K	±5%	.5w	Carbon Film
R2	1K	"	"	"
R3	1K	"	"	"
R4	1K	"	"	"
R5	1K	"	"	"
R6	1K	"	"	"
R7	1K	"	"	"
R8	1K	"	"	"
R9	390	"	"	"
R10	22K	"	"	"
R11	82K	"	"	"
R12	12K	"	"	"
R13	27K	"	"	"
R14	1M5	"	"	"
R15	6K8	"	"	"
R16	680	"	"	"
R17	1K	"	"	"
R18	560	"	"	"
R19	560	"	"	"
R20	1K	"	"	"
R21	8K2	"	"	"
R22	330	"	"	"
R23	1K	"	"	"

Circuit Ref.	Value μ Farads	Maximum Tolerance	Minimum Working Tolerance	Maker and Description
CAPACITORS				
C1	0.47	±10%	20v	**Mullard C281 - VV**
C2	1000p	±20%	20v	Wima Tropyfol F

Circuit Ref.	Type
TRANSISTORS	
TR1	BSX19
TR2	BC107
TR3	BC107
TR4	BSY41
TR5	BC107
TR6	BC107
DIODES	
D1	IN4148
D2	IN4148

5.3 COMPONENT LIST - LOGIC BOARD 2 continued

Circuit Ref.	Type
INTEGRATED CIRCUITS	
IC1	D930
IC2	D962
IC3	D946
IC4	D9306
IC5	D9306
IC6	D962
IC7	D936
IC8	D946
IC9	D962
IC10	D930
IC11	D946
IC12	D946
IC13	D946
IC14	D936
IC15	D946
IC16	D936
IC17	D9093
IC18	D930
IC19	D962
IC20	D936
IC21	D946
IC22	D946
IC23	D946
IC24	D9093
IC25	D962
IC26	D936
IC27	D9093
IC28	D9093
IC29	D936
IC30	D930
IC31	D962
IC32	D936

5.4 COMPONENT LIST - LOGIC BOARD 3

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R1	1K	±5%	.5W	Carbon Film
R2	1K	"	"	"
R3	1K	"	"	"
R4	1K	"	"	"
R5	Not used			
R6	1K	"	"	"
R7	1K	"	"	"
R8	1K	"	"	"
R9	Not used			
R10	1K	"	"	"
R11	1K	"	"	"
R12	1K	"	"	"
R13	1K	"	"	"

Circuit Ref.	Value u Farads	Maximum Tolerance	Minimum Working Voltage	Maker and Description
CAPACITORS				
C1	470p	±20%	10v	Wima Tropyfol F

Circuit Ref.	Type	Circuit Ref.	Type
DIODES			
D1	IN4148		
INTEGRATED CIRCUITS			
IC1	D936	IC13	D9093
IC2	D936	IC14	D962
IC3	D9308	IC15	D930
IC4	D9308	IC16	D9324
IC5	D936	IC17	D9324
IC6	D930	IC18	D9093
IC7	D946	IC19	D962
IC8	D946	IC20	D946
IC9	D946	IC21	D930
IC10	D946	IC22	D936
IC11	D946	IC23	D930
IC12	D9093		

5.5 COMPONENT LIST - LOGIC BOARD 4 - Type 1A only

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R1	2K7	±5%	.5w	Carbon Film
R2	2K7	"	"	"
R3	2K7	"	"	"
R4	2K7	"	"	"
R5	2K7	"	"	"
R6	2K7	"	"	"
R7	2K7	"	"	"
R8	1K	"	"	"
R9	390	"	"	"
R10	6K8	"	"	"
R11	6K8	"	"	"
R12	6K8	"	"	"
R13	6K8	"	"	"
R14	6K8	"	"	"
R15	6K8	"	"	"
R16	6K8	"	"	"
R17	6K8	"	"	"
R18	5K6	"	"	"
R19	5K6	"	"	"
R20	1K	"	"	"
R21	1K	"	"	"
R22	1K	"	"	"
R23	1K	"	"	"
R24	5K6	"	"	"
R25	5K6	"	"	"
R26	5K6	"	"	"
R27	5K6	"	"	"
R28	5K6	"	"	"
R29	100	"	"	"
R30	1K	"	"	"
R31	1K	"	"	"

Circuit Ref.	Value μ Farads	Maximum Tolerance	Minimum Working Voltage	Maker and Description
CAPACITORS				
C1	1500p	±10%	10v	Wima Tropyfol F

Circuit Ref.	Type
TRANSISTORS	
TR1	BC107
TR2	BC107

5.5 COMPONENT LIST - LOGIC BOARD 4 - Type 1A only continued

Circuit Ref.	Type
INTEGRATED CIRCUITS	
IC1	D946
IC2	D936
IC3	D946
IC4	D9093
IC5	D9093
IC6	DM8810
IC7	DM8810
IC8	D9093
IC9	D936
IC10	D9093
IC11	D946
IC12	D9093
IC13	D9093
IC14	MM5220GJ
IC15	D946
IC16	D962
IC17	D936
IC18	D930
IC19	D936
IC20	D9312
IC21	D946
IC22	D936
IC23	D932
IC24	D9324
IC25	D9310
IC26	D962
IC27	D9093

5.6 COMPONENT LIST - LOGIC BOARD 5 - Type 1A only

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R1	1K	±5%	.5w	Carbon Film
R2	1K	"	"	"
R3	1K	"	"	"
R4	1K	"	"	"
R5	1K	"	"	"
R6	1K	"	"	"
R7	1K	"	"	"
R8	5K6	"	"	"
R9	5K6	"	"	"
R10	5K6	"	"	"
R11	1K	"	"	"
R12	1K	"	"	"
R13	3K3	"	"	"
R14	18K	"	"	"
R15	1K	"	"	"
R16	1K	"	"	"
R17	1K	"	"	"
R18	1K	"	"	"
R19	100	"	"	"
R20	1K	"	"	"

Circuit Ref.	Value μ Farads	Maximum Tolerance	Minimum Working Voltage	Maker and Description
CAPACITORS				
C1	0.01	±20%	10v	Wima Tropyfol F

Circuit Ref.	Type
TRANSISTORS	
TR1	BSX19
DIODES	
D1	IN4148
D2	IN4148
D3	IN4148
D4	IN4148
D5	IN4148
D6	IN4148

5.6 COMPONENT LIST - LOGIC BOARD 5 - Type IA only continued

Circuit Ref.	Type
INTEGRATED CIRCUITS	
IC1	D9093
IC2	D9093
IC3	D932
IC4	D9093
IC5	D9093
IC6	D9093
IC7	D9310
IC8	D9310
IC9	D9310
IC10	D9093
IC11	D946
IC12	D932
IC13	D946
IC14	D962
IC15	D9093
IC16	D9324
IC17	D9312
IC18	D9312
IC19	D946
IC20	D936
IC21	D946
IC22	D936
IC23	D946
IC24	D9310
IC25	D9312
IC26	D9312
IC27	D946
IC28	D962
IC29	D936
IC30	D962
IC31	D936
IC32	D9310
IC33	D9310
IC34	D9310
IC35	D946

5.7 COMPONENT LIST - SUB BOARD

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R1	47	±5%	.5w	Carbon Film
R2	10K	"	"	"
R3	22K	"	"	"
R4	8K2	±2%	1w	**Electrosil TR6**
R5	1K	±5%	.5w	Carbon Film
R6	1K	"	"	"
R7	150	"	"	"
R8	1K	"	"	"
R9	10K	"	"	"
R10	47	"	"	"
R11	10K	"	"	"
R12	330	"	"	"
R13	3K9	"	"	"
R14	Not used			
R15	Not used			
R16	10K	"	"	"
R17	8K2	±2%	1w	**Electrosil TR6**
R18	47	±5%	.5w	Carbon Film
R19	22K	"	"	
R20	10K	"	"	"
R21	680	"	"	"
R22	470	"	"	"
R23	470	"	"	"
R24	Not used			
R25	330	"	"	"
R26	3K9	"	"	"
R27	22K	"	"	"
R28	Not used			
R29	Not used			
R30	Not used			
R31	6K8	"	"	"
R32	A.O.T.	"	"	"
R33	2K2	"	"	"
R34	820	"	"	"
R35	10K	"	"	"
R36	150	"	"	"
R37	27K	"	"	"
R38	2K2	"	"	"
R39	A.O.T.	"	"	"
R40	6K8	"	"	"
R41	47	"	"	"
R42	22K	"	"	"
R43	820	"	"	"
R44	4K7	"	"	"
R45	27K	"	"	"
R46	3K3	"	"	"
R47	A.O.T.	"	"	"
R48	6K8	"	"	"
R49	1K8	"	"	"

5.7 COMPONENT LIST - SUB BOARD continued

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R50	1K	±5%	.5w	Carbon Film
R51	Not used			
R52	Not used			
R53	Not used			
R54	Not used			
R55	1K2	"	"	"
R56	10K	"	"	"
R57	3K3	"	"	"
R58	680	"	"	"
R59	1K	"	"	"
R60	680	"	"	"
R61	680	"	"	"
R62	12K	"	"	"
R63	1K	"	"	"

Circuit Ref.	Value µ Farads	Maximum Tolerance	Minimum Working Voltage	Maker and Description
CAPACITORS				
C1	0.1	±20%	250v	Mullard C281 VV
C2	0.1	"	40v	"
C3	A.O.T.	"		Erie HI-K AD
C4	0.1	"	40v	Mullard C281 VV
C5	0.1	"	250v	"
C6	A.O.T.	"	200v	Erie HI-K AD
C7	A.O.T.	"	200v	"
C8	0.1	"	20v	Wima Tropyfol M
C9	100	+50% -20%	10v	Printilyt
C10	100	"	"	"
C11	0.1	±20%	40v	Mullard C281 VV
C12	A.O.T.	"	200v	Erie HI-K AD
C13	A.O.T.	"	200v	"
C14	Not used			
C15	.01	"	500v	Erie HI-K Style 811

Circuit Ref.	Type
TRANSISTORS	
TR1	BF258
TR2	BC107
TR3	BC107
TR4	BF258
TR5	BC107
TR6	BF258
TR7	BC107
TR8	BC107
TR9	BF258
TR10	BC107

5.7 COMPONENT LIST - SUB BOARD continued

Circuit Ref.	Type
TRANSISTORS	
TR11	BCY70
TR12	BC107
TR13	BCY70
TR14	BC107
TR15	BC107
TR16	BCY70
TR17	BC107
TR18	BC107
TR19	BF258
TR20	BSX19
TR21	BSX19
TR22	BSX19
TR23	BSX19
TR24	BSX19
DIODES	
D1	IN4148
D2	IN4148
D3	IN4148
D4	IN4148

5.8 COMPONENT LIST - E.H.T. BOX ASSEMBLY

5.8.1 E.H.T. BOX ASSEMBLY

Circuit Ref.	Type/Maker
L1	Bobbin to Trend Drg. AKJ 5450A
L2	Bobbin to Trend Drg. AKJ 5451A

5.8.2 E.H.T. BOARD ASSEMBLY

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R1	A.O.T.	±5%	½w	Carbon Film
R2	12K	"	"	"
R3	10	"	"	"
R4	2.2M	"	"	"
R5	820K	"	"	"

Circuit Ref.	Value µ Farads	Maximum Tolerance	Minimum Working Voltage	Maker and Description
CAPACITORS				
C1	10	-20% +50%	30v	Elkmold TCC
C2	0.047	±20%	30v	Mullard C281
C3	1.0	"	30v	STC Tag
C4	0.01	"	500v	Erie Nax Transcap
C5	0.01	"	500v	Erie Nax Transcap

Circuit Ref.	Type
DIODES	
D1	SCM 10
D2	SCM 10

5.8.3 TAG BOARD ASSEMBLY

Circuit Ref.	Value µ Farads	Maximum Tolerance	Minimum Working Voltage	Maker and Description
CAPACITORS				
C6	220p	±20%	5KV	Radiospares Disc
C7	220p	"	"	"
C8	220p	"	"	"
C9	220p	"	"	"

5.8 COMPONENT LIST - E.H.T. BOX ASSEMBLY continued

5.8.3 TAG BOARD ASSEMBLY continued

Circuit Ref.	Type
DIODES	
D3	SCM 40
D4	SCM 40
D5	SCM 40
D6	SCM 40
MISCELLANEOUS	
PL12	Plug Cinch 43/81/043 with Shroud 43/81/960
	Nylon Screw M3 CH.HD. 8mm long
EHT Connector	Cinch P71 81133 00 000
EHT Shroud	Cinch P71 77529 00 000

5.9 COMPONENT LIST - REAR AND SIDE PANEL ASSEMBLY

5.9.1 REAR PANEL

Circuit Ref.	Value ohms	Maker and Description
RESISTOR VARIABLE		
RV1	1K	Bourns 3852 A-202-102A
RV2	25K	Bourns 3852 A-202-253A

Circuit Ref.	Type
TRANSISTORS	
	2N3055 with Insulating Kit
	2N3055 with Insulating Kit
DIODES	
	BYX-42-300 with Insulating Kit
	BYX-42-300 with Insulating Kit

Circuit Ref.	Item	Type/Maker
MISCELLANEOUS		
	Fuseholder	Belling-Lee L2006
FS1	Fuselink	1A Delay size 20 x 5mm Standard Fuse Co.
SKT9	Socket	Miniature 3 Pole Belling-Lee L1950
SKT8	Socket	25-way Cinch 43/81/048
	Base Assy.	25-way Cinch 43/81/965
	Voltage Selector	Cinch R80-81118-00-000-Red Plug
SW16	Switch Rotary	2 Pole 2 Position Trend Drawing AKJ 5219-C
SW14	Switch Rotary	3 Pole 10 Position Trend Drawing AKJ 7440-C - Type 1A only
SW15	Switch Rotary	1 Pole 3 Position Trend Drawing AKJ 5434-C - Type 1A only
	Barb Sockets	White 5156 Oxley

5.9 COMPONENT LIST - REAR AND SIDE PANEL ASSEMBLY continued

5.9.2 SIDE PANEL

Circuit Ref.	Value ohms	Tolerance	Rating	Maker/Type
RESISTORS				
R1	820	5%	2w	Electrosil TR8
R2	820	5%	2w	Electrosil TR8
R3	1K	±10%	10w	Welwyn
R51	6K8	±10%	6w	W/W type Welwyn
R52	5K6	±10%	6w	W/W type Welwyn

Circuit Ref.	Value μ Farads	Tolerance	Working Voltage	Make and Description
CAPACITOR				
C1	50 + 50	-10% +50%	275v	Hunts L38/2
C2	2200	"	40v	Mullard 07117222
C3	2200	"	25v	Mullard 07116222
C4	2200	"	25v	Mullard 07116222
C5	4700	"	10v	Mullard 07114472
C6	4700	"	10v	Mullard 07114472

Circuit Ref	Type
DIODES	
D1-D10	BYX 36 300

Circuit Ref.	Item	Type and Maker
MISCELLANEOUS		
T1	Transformer	Trend Drg. No. AKJ 4653C
SKT10	Socket	23-way Painton 74/10/2355/10
SKT11	Socket	Belling-Lee L1387/S/Ag
	Shroud	Belling-Lee L1470/F
	Filter Assy	Trend Drg. No. AKB 7643-A
S1-3	Plug Type 40P/156	Oxley Dev Ltd.
	Socket Type 40S/156	Oxley Dev Ltd.
	17 way Edge Connector	Trend Drg. No. AKJ 5598-A
	Oscilloscope Tube	D10-210 x 15 Thorn
	Mu-Metal Shield	Magnetic Shield
	Twist Coil	T24 Vere Eng.

5.10 COMPONENT LIST - FRONT PANEL ASSEMBLY

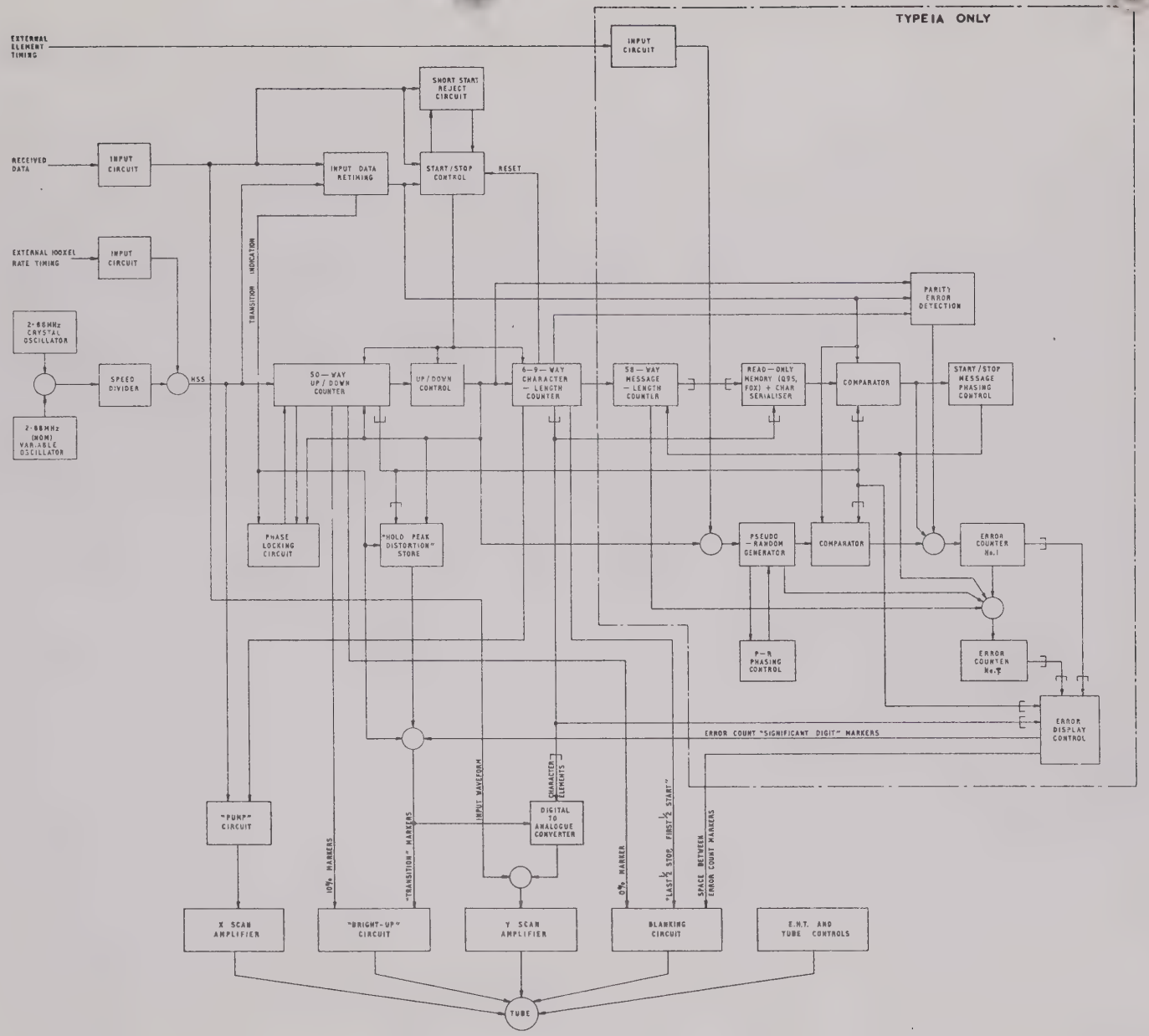
Circuit Ref.	Description	Type/Maker
SWITCHES		
SW1	Toggle	Waycom MST 216N
SW2	Lever 2 Pole 4 Position	Trend Drg. No. AKJ 5233C
SW3	Toggle	Waycom MST 116D
SW4	Toggle	Waycom MST 116D
SW5	Lever 2 Pole 4 Position	Trend Drg. No. AKJ 5233C
SW6	Wafer 3 Pole 5 Position	Trend Drg. No. AKJ 5187C
SW7	Lever 1 Pole 3 Position	Trend Drg. No. AKB 4408C
SW8	Lever 2 Pole 4 Position	Trend Drg. No. AKJ 5233C
SW9	Wafer 2 Pole 11 Position	Trend Drg. No. AKJ 5259C
SW10	Toggle	Waycom MST 116D
SW11	Toggle	Waycom MST 116D
SW12	Wafer 1 Pole 7 Position	Trend Drg. No. AKJ 5188C (Not used on Type II)
SW13	Lever 1 Pole 3 Position	Trend Drg. No. AKJ 5230C
PB1	Miniature	Arcolectric T906
PB2	Miniature	Arcolectric T906

Circuit Ref.	Type/Maker
POTENTIOMETERS	
RV1	3852C-161-105A Bourns
RV2	3852C-161-503A Bourns
RV3	3852C-161-105A Bourns
RV4	Trimpot Type CW 52M
RV5	Trimpot Type CW 52M
RV6	250 ohm MW Reliance
INDICATORS	
LP1	Neon Indicator L1902 240v Red. Belling-Lee
LP2	Solid State Lamp 5082-4440 Hewlett Packard
LP3	" " "
LP4	" " "
	(LP4 not used on Type 2A)
TERMINALS	
T1-4	4mm Socket Radiall 941-420
	Modified Edge Connector AKB 4799-A

Circuit Ref.	Value ohms	Tolerance	Rating	Type
RESISTORS				
R1	270K	5%	.5w	Carbon Film
R2	150	2%	$\frac{1}{4}$w	Electrosil TR4
R3	150	"	"	"
R4	150	"	"	"

5.10 COMPONENT LIST - FRONT PANEL ASSEMBLY continued

Circuit Ref.	Type/Maker
CONNECTORS	
	Painton 74/10/2301/10
MISCELLANEOUS	
	Filter AKJ 5468-A
KNOBS	
21mm - 3	70-21-$\frac{1}{4}$-Black Cap 1450-21/Grey 1451-21-Grey Pointer
14.5mm - 1	70-14-$\frac{1}{4}$-Black Cap 1450-14/Grey 1451-24-Grey Pointer
10mm - 3	70-10-$\frac{1}{8}$-Black Cap 1450- 9/Grey 1451-10-Grey Pointer
Cambion Plug 3308/1/03	Belling-Lee Socket 1387/S/Ag



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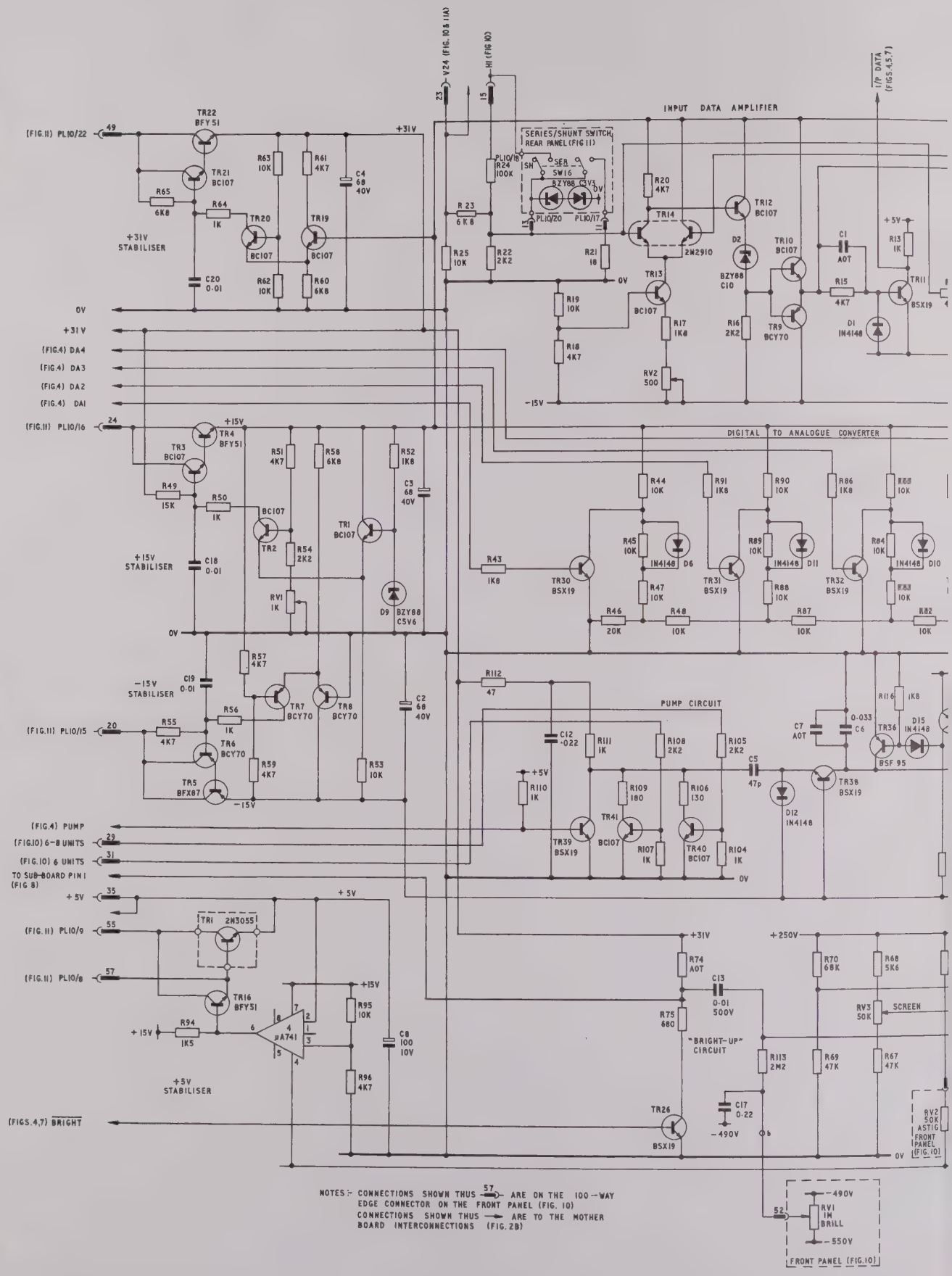
BLOCK SCHEMATIC DIAGRAM

FIG. 1



NOTES:- CONNECTIONS SHOWN THUS 57 ARE ON THE 100-WAY EDGE CONNECTOR ON THE FRONT PANEL (FIG. 10)
CONNECTIONS SHOWN THUS → ARE TO THE MOTHER BOARD INTERCONNECTIONS (FIG. 28)

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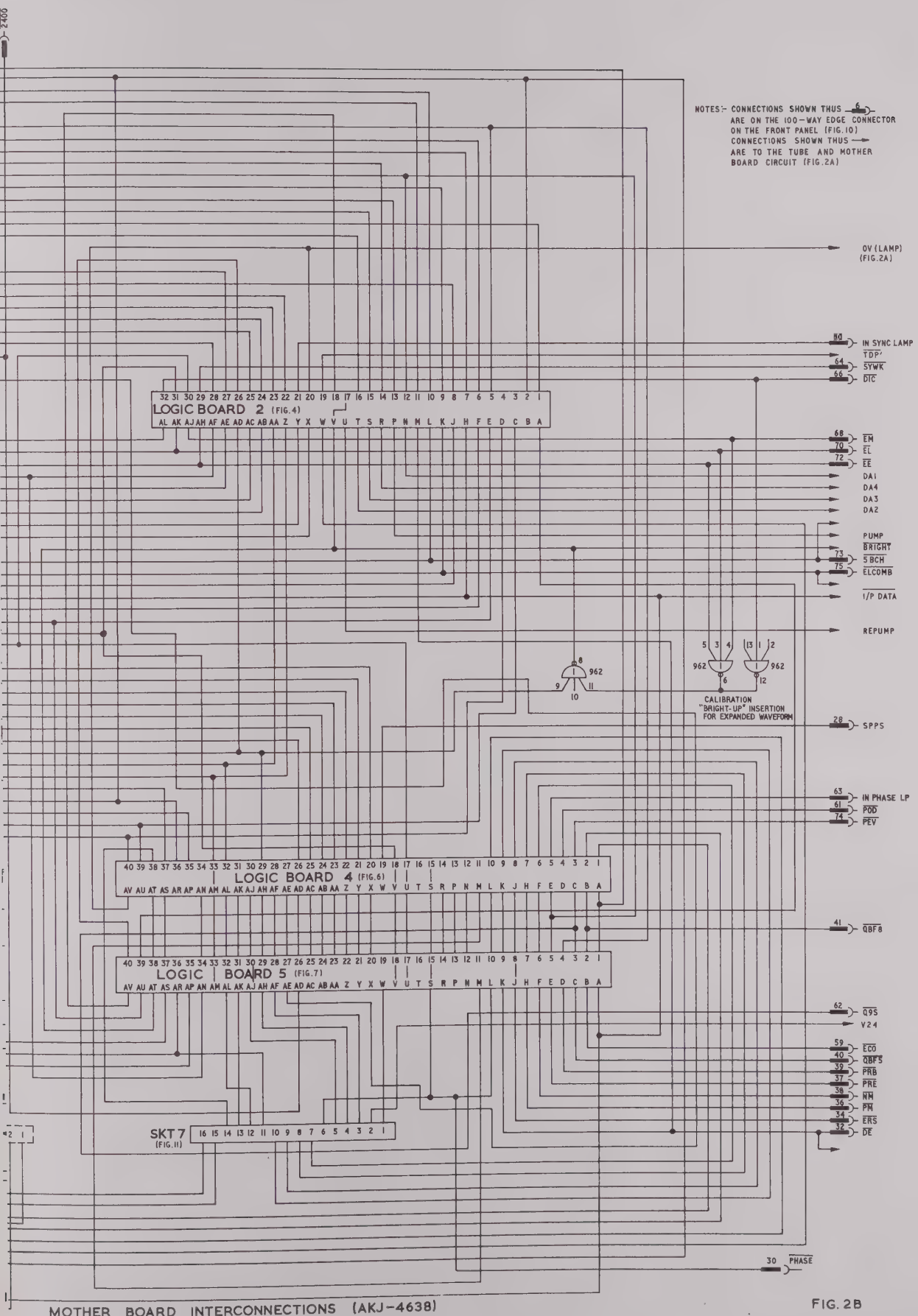
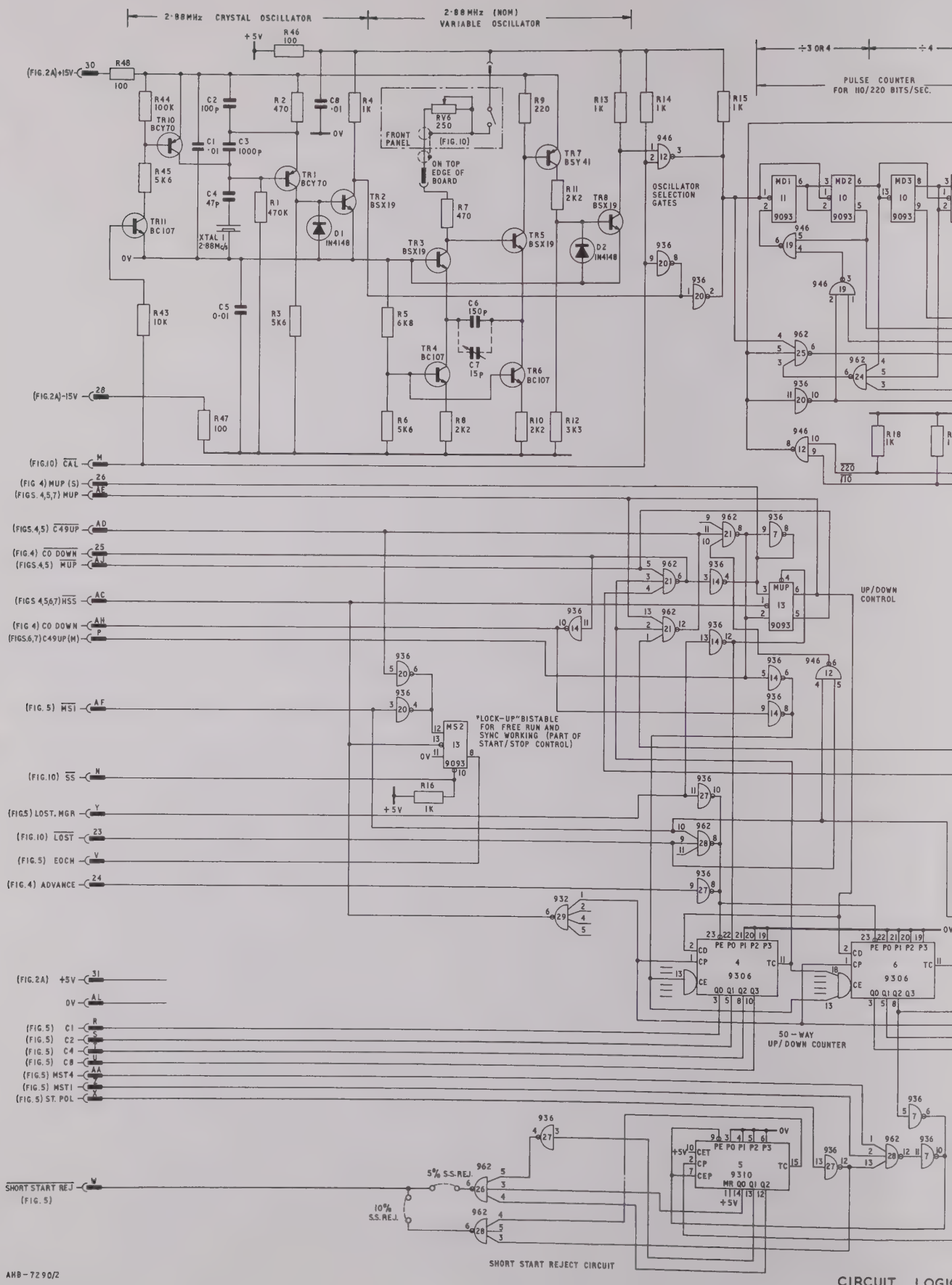
TUBE AND MOTHER BOARD CIRCU



MOTHER BOARD INTERCONNECTIONS (AKJ-4638)

FIG. 2B



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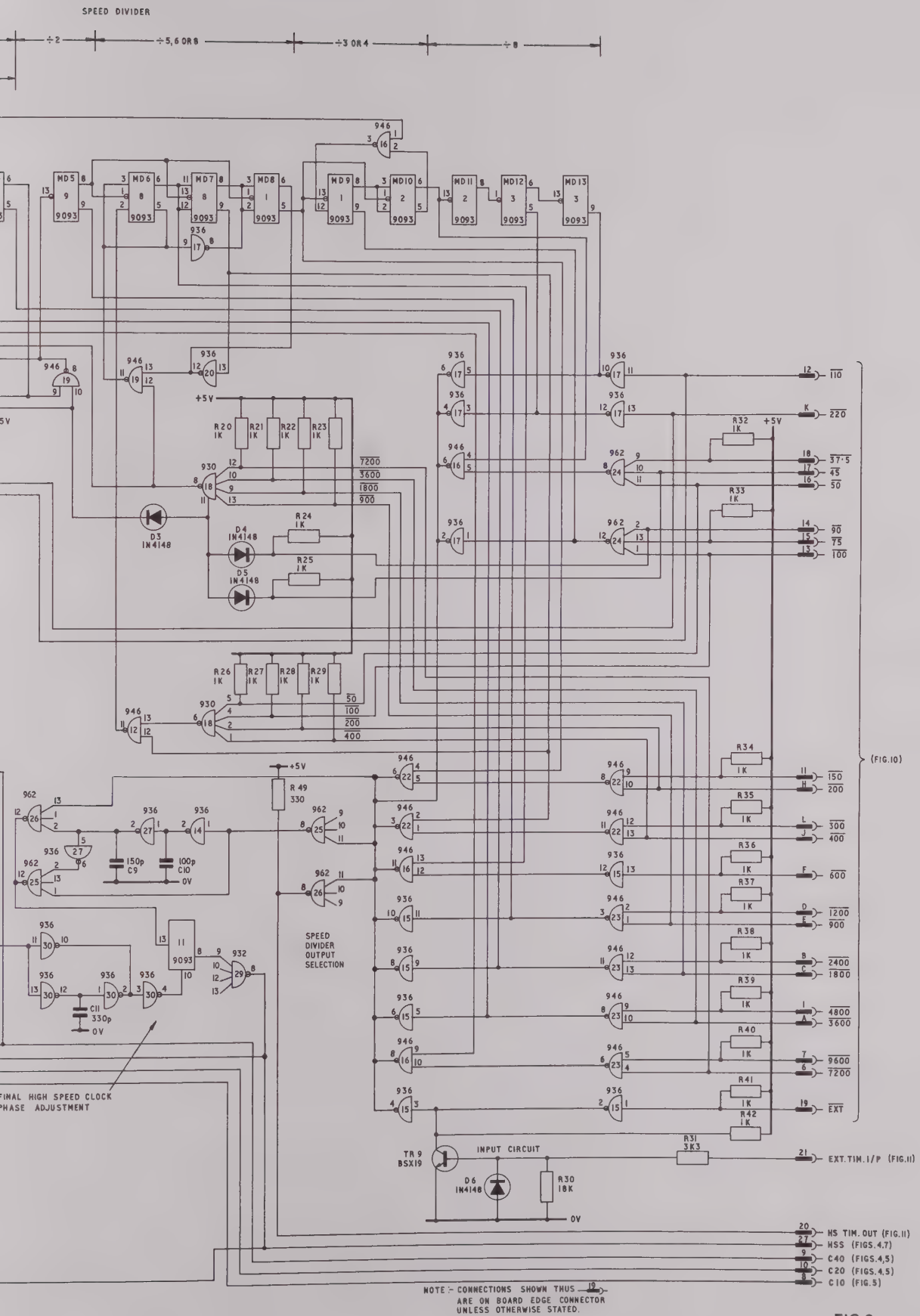
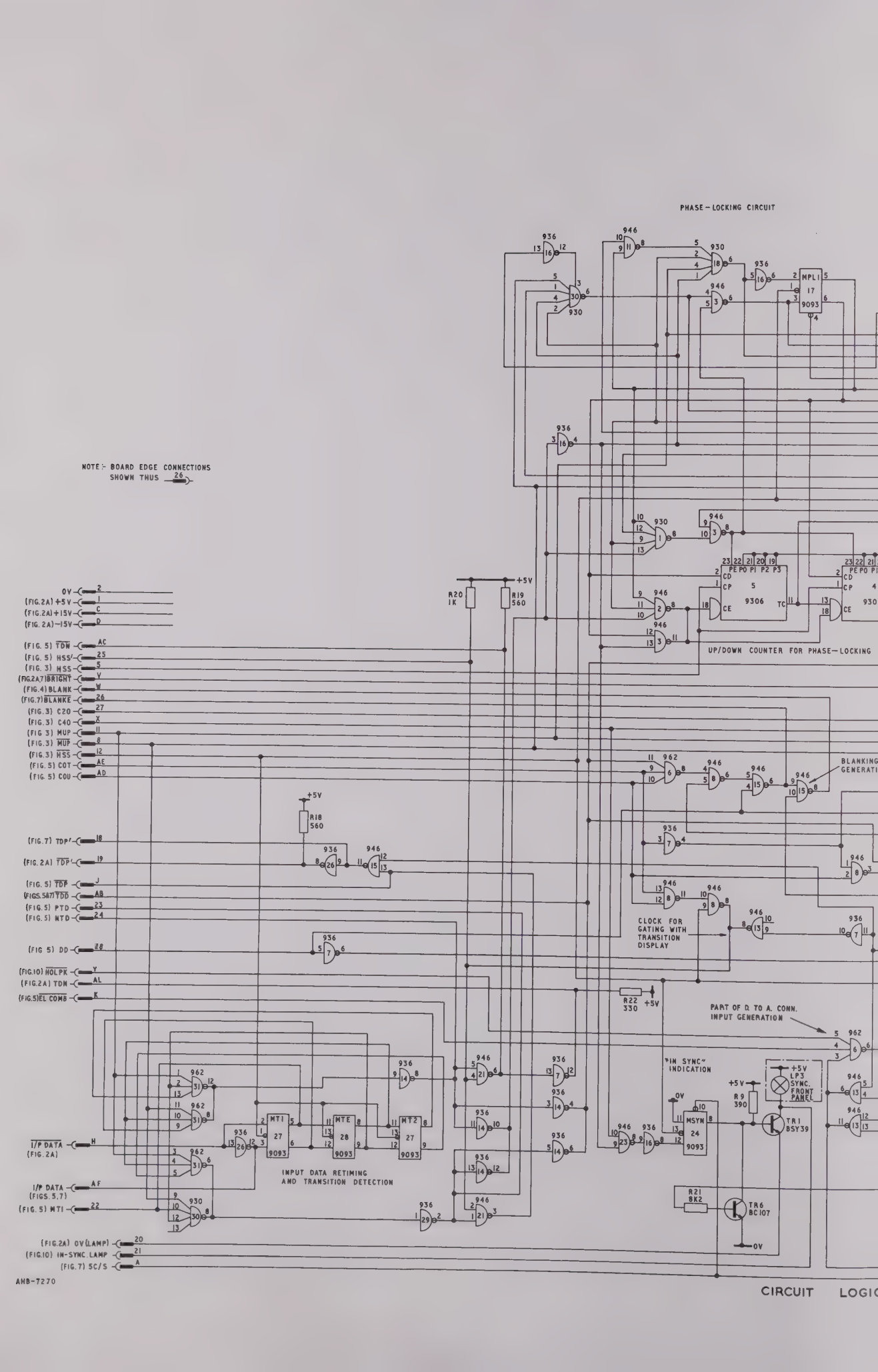
CIRCUIT LOGI

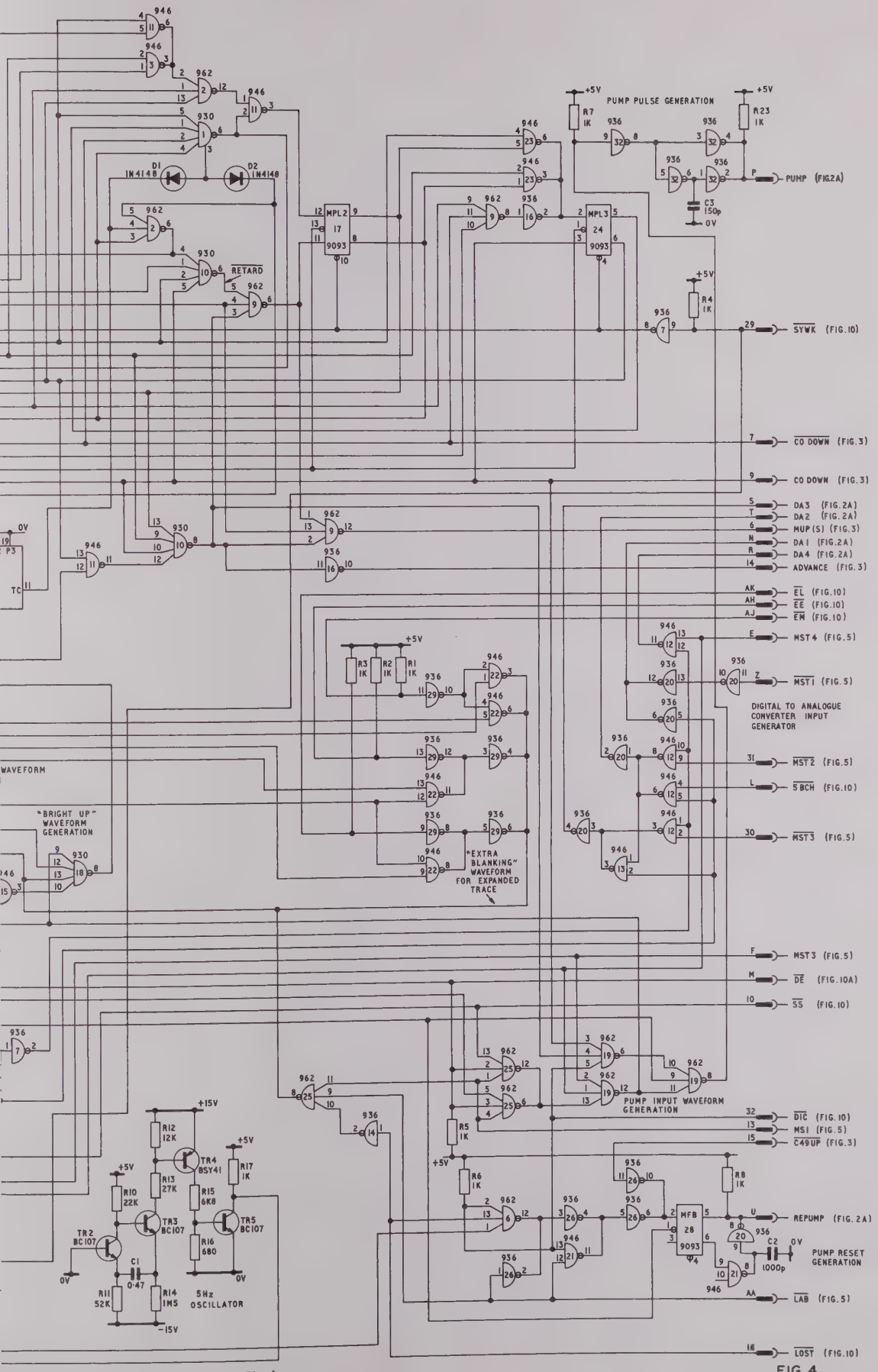


NOTE :- CONNECTIONS SHOWN THUS —12— ARE ON BOARD EDGE CONNECTOR UNLESS OTHERWISE STATED.

BOARD 1. (ASS'Y. No. AKJ-7291)

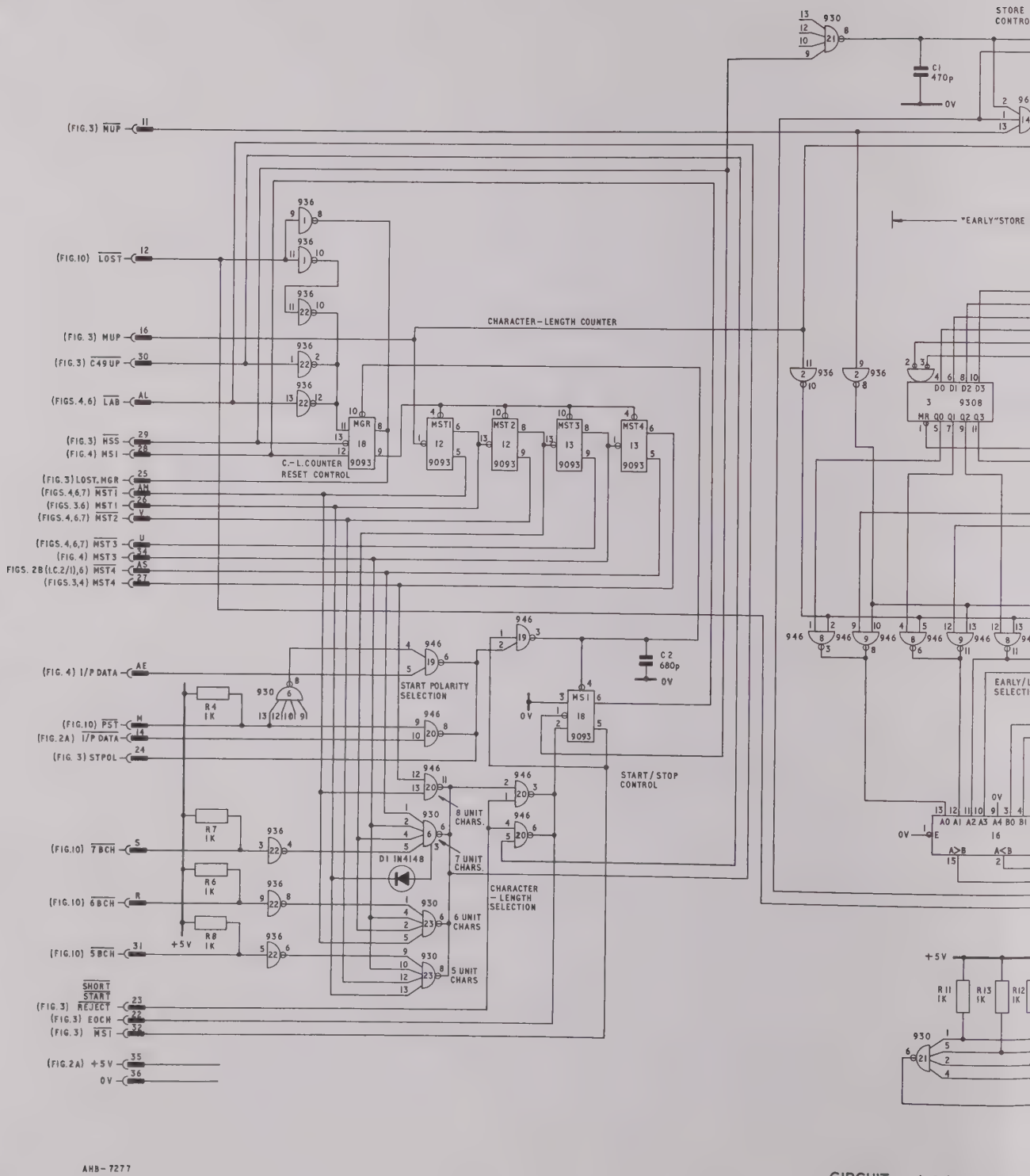
FIG. 3


PHASE – LOCKING CIRCUIT
NOTE :- BOARD EDGE CONNECTIONS SHOWN THUS 26
UP/DOWN COUNTER FOR PHASE–LOCKING
CLOCK FOR GATING WITH TRANSITION DISPLAY
PART OF D. TO A. CONN. INPUT GENERATION
"IN SYNC" INDICATION
INPUT DATA RETIMING AND TRANSITION DETECTION
0V
(FIG.2A) +5V
(FIG.2A) +15V
(FIG. 2A) –15V
(FIG. 5) TDW
(FIG. 5) HSS'
(FIG. 3) HSS
(FIG.2A,7) BRIGHT
(FIG.4) BLANK
(FIG.7) BLANKE
(FIG.3) C20
(FIG.3) C40
(FIG 3) MUP
(FIG.3) MUP
(FIG.3) HSS
(FIG. 5) COT
(FIG. 5) COU
(FIG.7) TDP'
(FIG. 2A) TDP'
(FIG. 5) TDP
(FIGS. 5&7) TDD
(FIG. 5) PTD
(FIG. 5) NTD
(FIG 5) DD
(FIG.10) HOLPK
(FIG.2A) TDN
(FIG.5) EL COMB
I/P DATA (FIG. 2A)
I/P DATA (FIGS. 5,7)
(FIG. 5) MTI
(FIG.2A) 0V (LAMP)
(FIG.10) IN-SYNC. LAMP
(FIG. 7) SC/S
R20 1K
R19 560
R18 560
R22 330
R9 390
R21 8K2
TR1 BSY39
TR6 BC107
LP3 SYNC. FRONT PANEL
AMB-7270
CIRCUIT LOGIC



BOARD 2 (ASS'Y. No. AKJ-7271)

FIG. 4



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CIRCUIT LOGIC BOAR

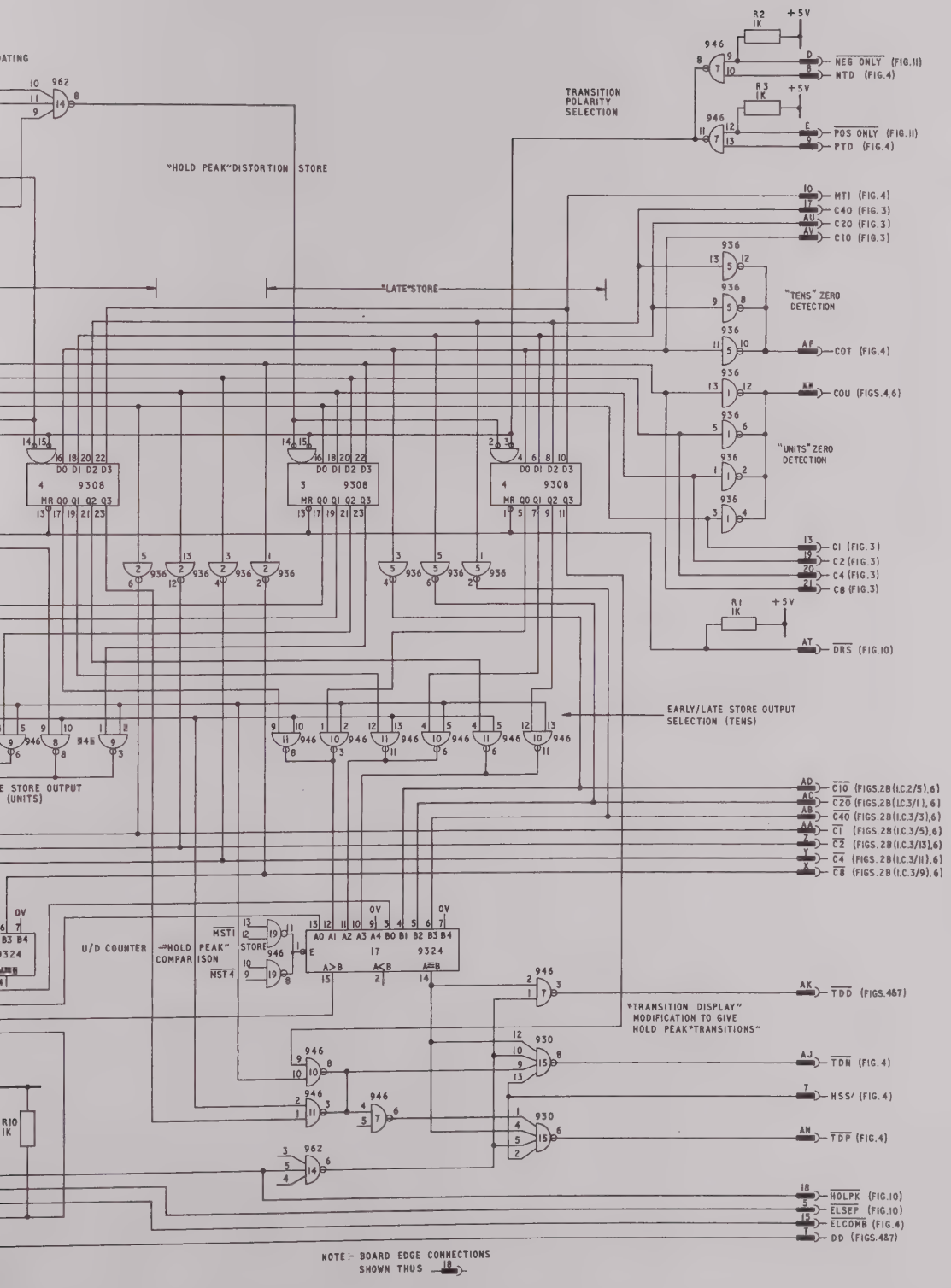
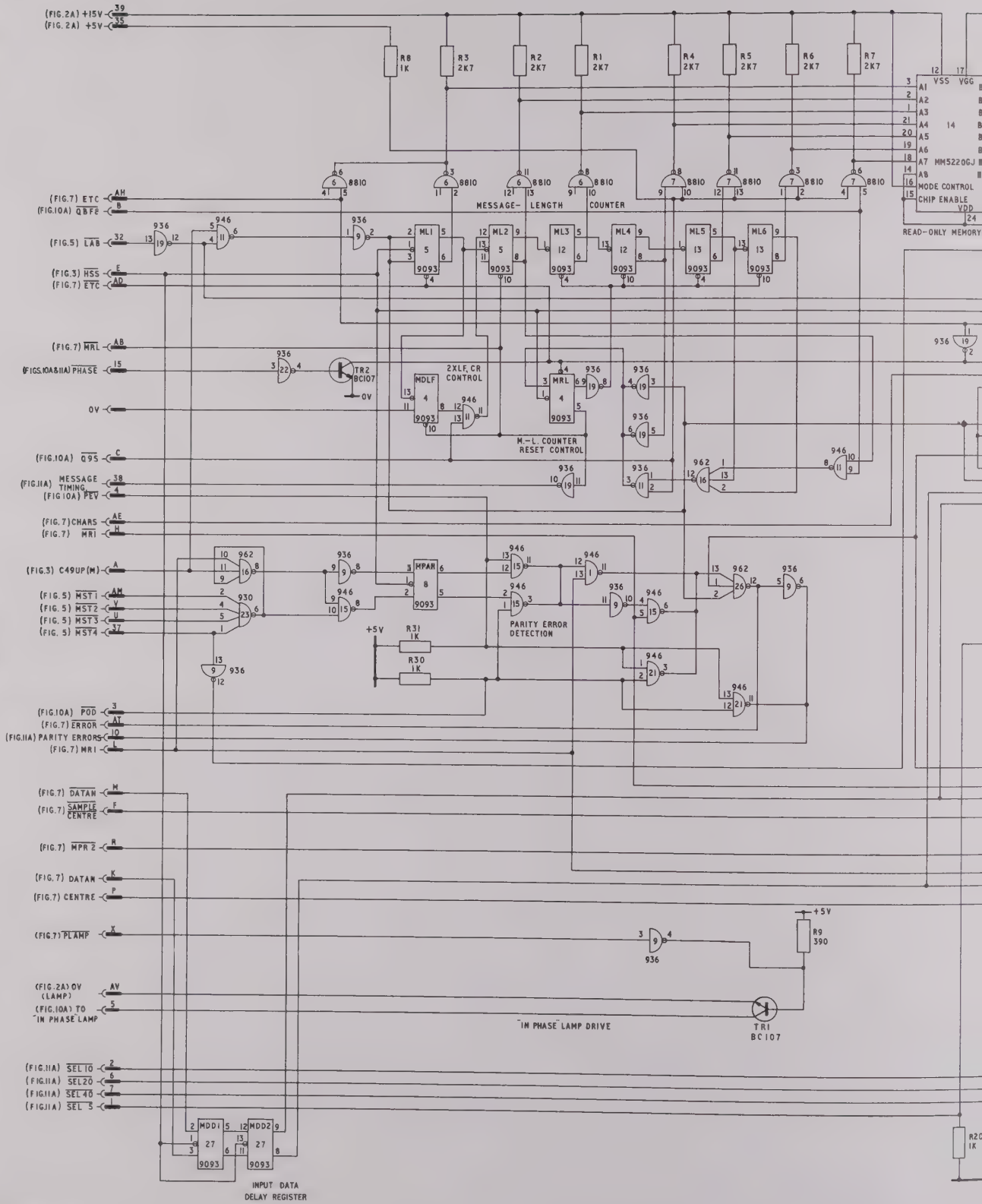

TRANSITION POLARITY SELECTION
"HOLD PEAK" DISTORTION STORE
"LATE" STORE
"TENS" ZERO DETECTION
"UNITS" ZERO DETECTION
EARLY/LATE STORE OUTPUT SELECTION (TENS)
U/D COUNTER
"HOLD PEAK" COMPARISON
"TRANSITION DISPLAY" MODIFICATION TO GIVE HOLD PEAK "TRANSITIONS"
NOTE :- BOARD EDGE CONNECTIONS SHOWN THUS

FIG.5



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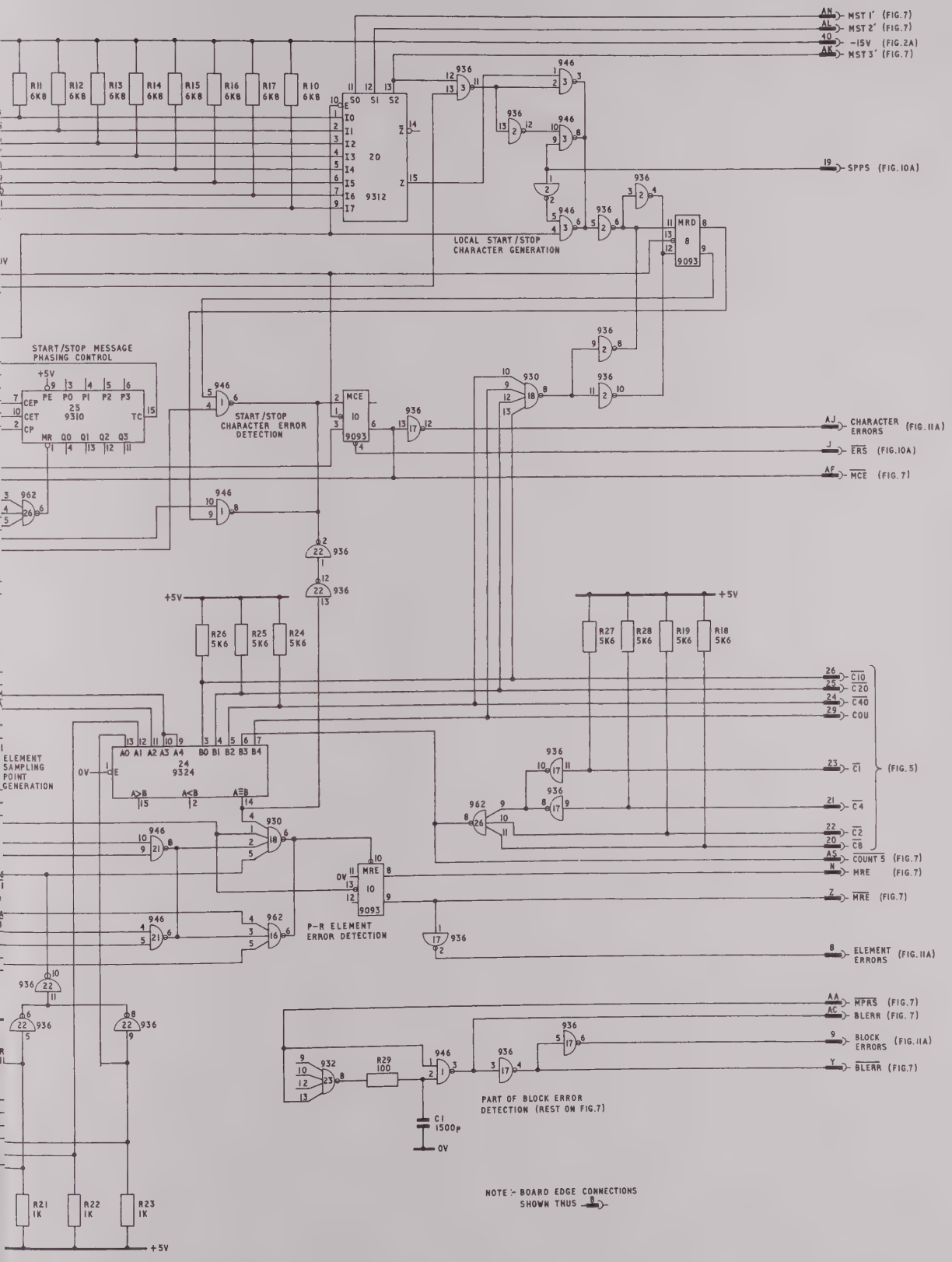
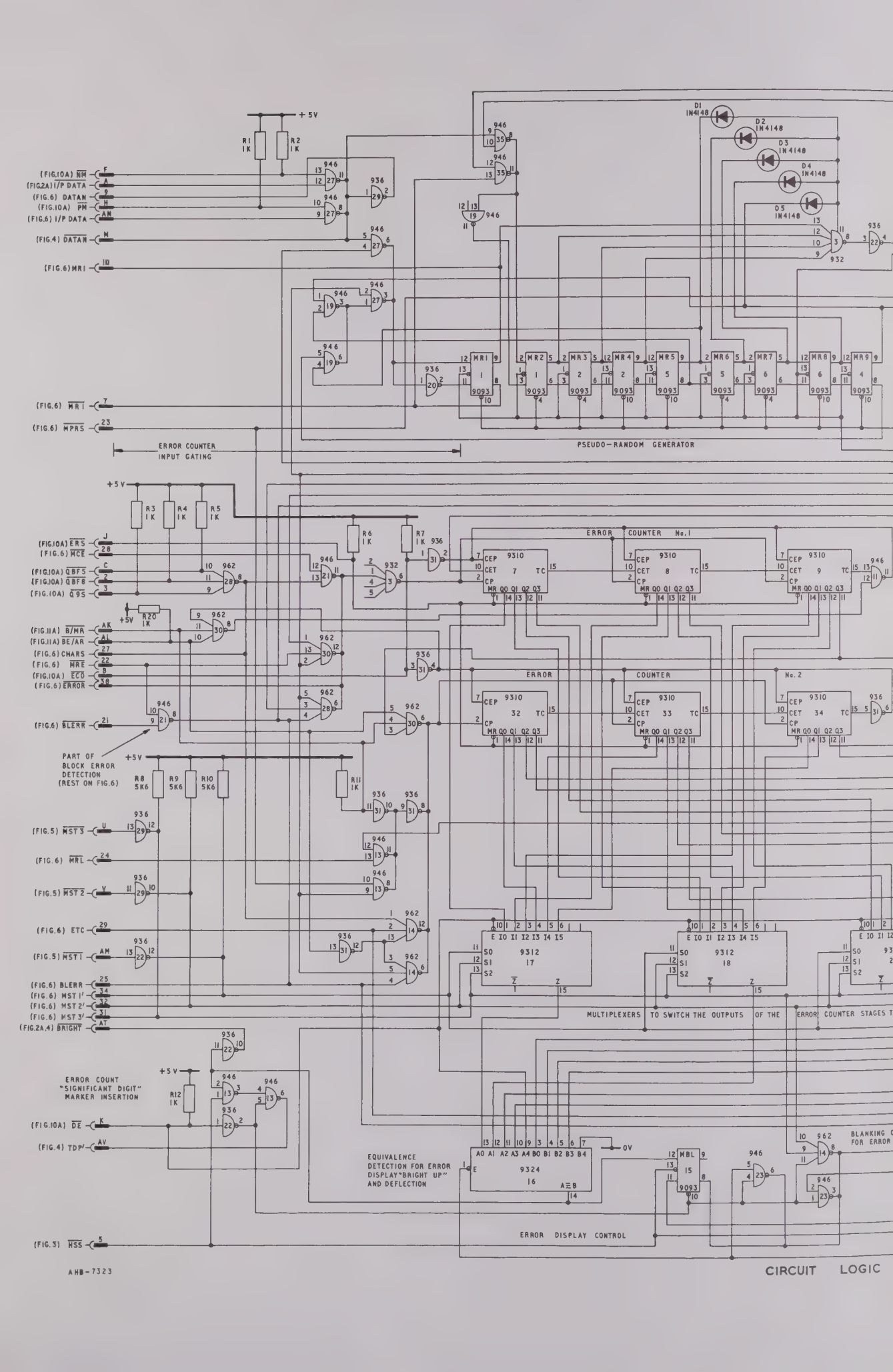
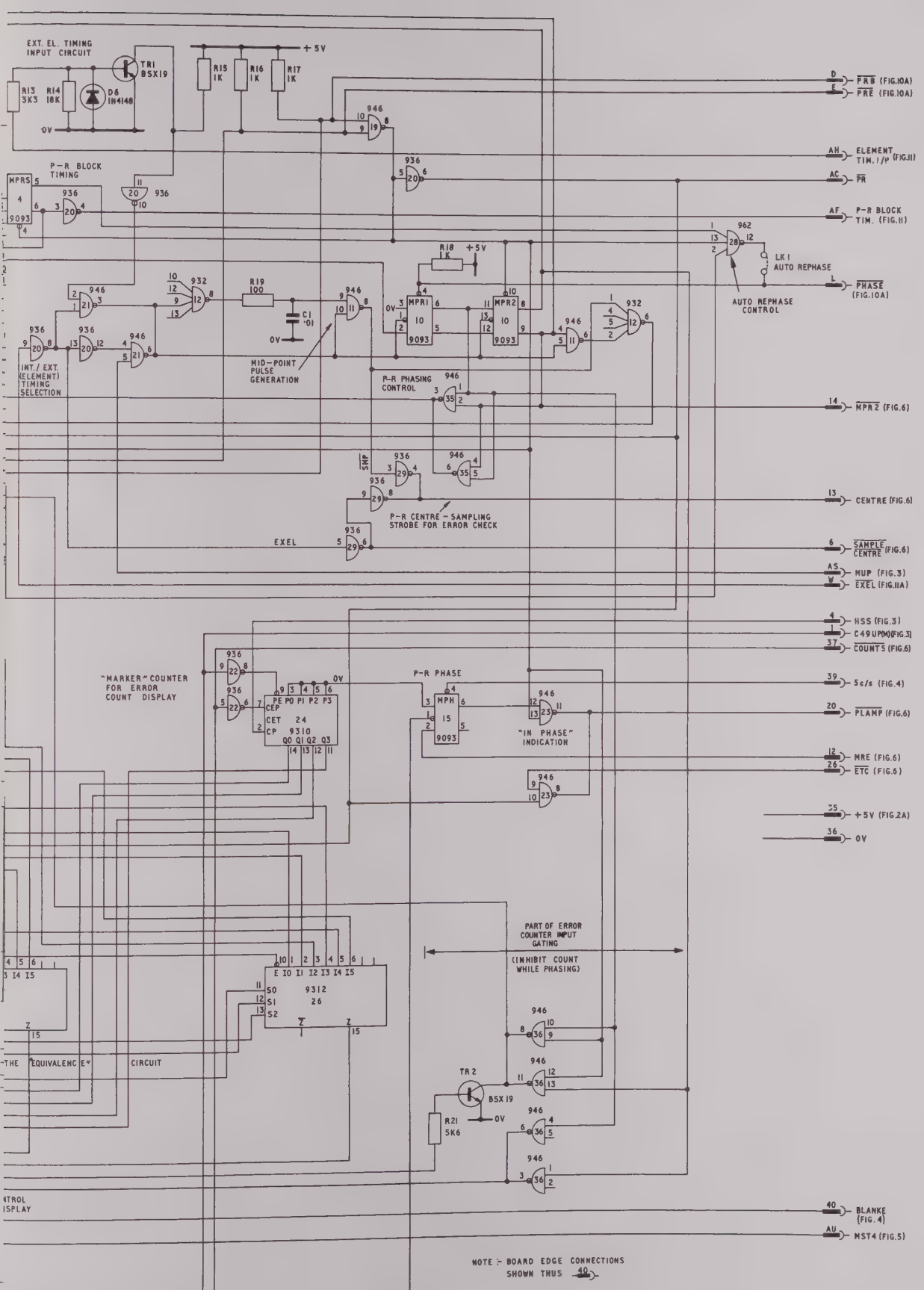
CIRCUIT LOGIC B



OARD 4. (ASSY. No. AKJ-4639)

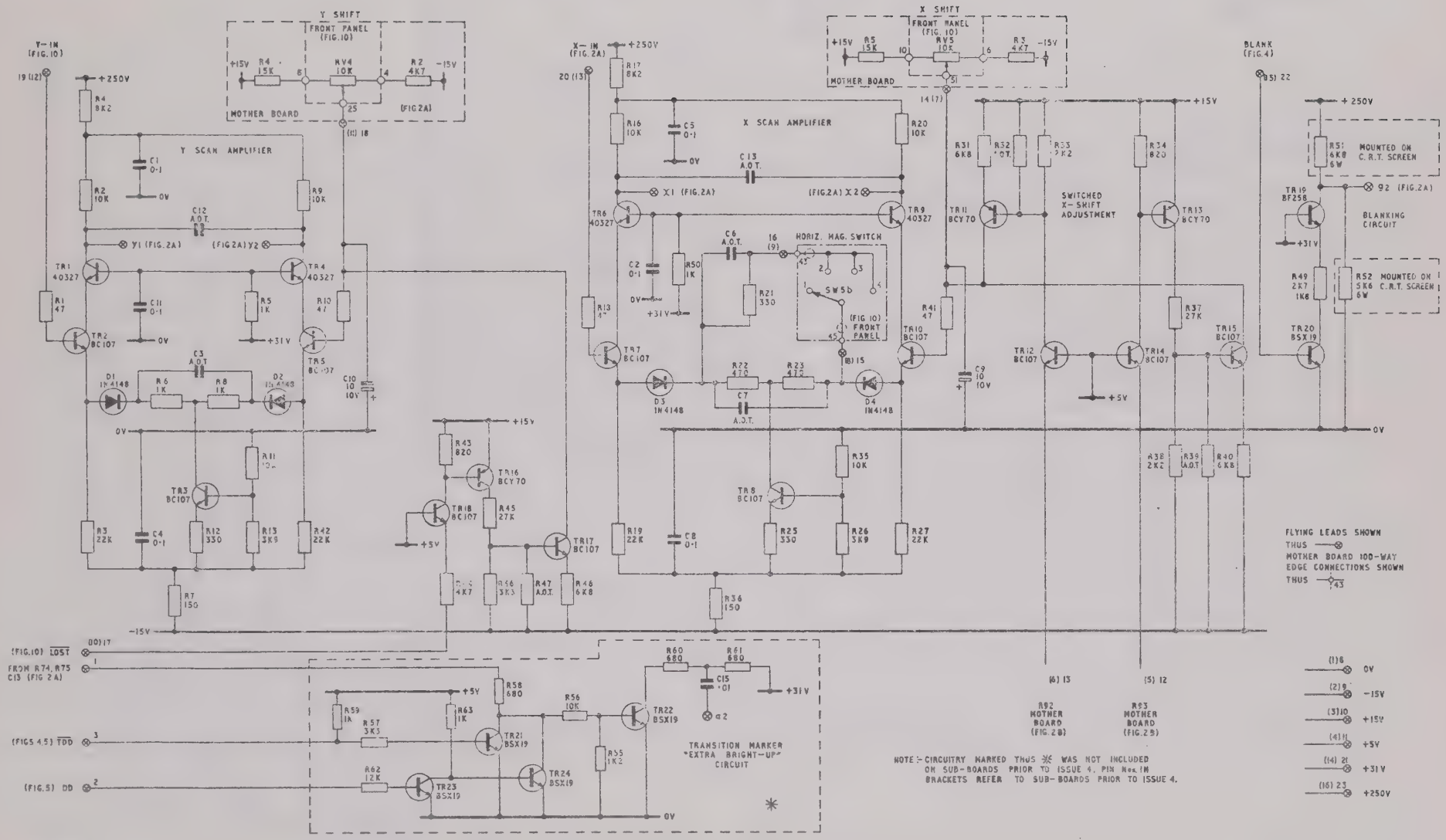
FIG.6


PSEUDO-RANDOM GENERATOR
ERROR COUNTER INPUT GATING
ERROR COUNTER No.1
ERROR COUNTER No.2
PART OF BLOCK ERROR DETECTION (REST ON FIG.6)
MULTIPLEXERS TO SWITCH THE OUTPUTS OF THE ERROR COUNTER STAGES T
ERROR COUNT "SIGNIFICANT DIGIT" MARKER INSERTION
EQUIVALENCE DETECTION FOR ERROR DISPLAY "BRIGHT UP" AND DEFLECTION
ERROR DISPLAY CONTROL
BLANKING FOR ERROR
AHB-7323
CIRCUIT LOGIC



OARD 5 (ASS'Y. No. (AKJ-7324)

FIG. 7


Y SHIFT
FRONT PANEL (FIG.10)
MOTHER BOARD
Y SCAN AMPLIFIER
Y-IN (FIG.10)
X SHIFT
FRONT PANEL (FIG. 10)
MOTHER BOARD
X SCAN AMPLIFIER
X-IN (FIG.2A)
BLANK (FIG.4)
SWITCHED X-SHIFT ADJUSTMENT
HORIZ. MAG. SWITCH
SW5b
(FIG 10) FRONT PANEL
MOUNTED ON C.R.T. SCREEN
BLANKING CIRCUIT
TRANSITION MARKER "EXTRA BRIGHT-UP" CIRCUIT
FLYING LEADS SHOWN THUS
MOTHER BOARD 100-WAY EDGE CONNECTIONS SHOWN THUS
NOTE:- CIRCUITRY MARKED THUS * WAS NOT INCLUDED ON SUB-BOARDS PRIOR TO ISSUE 4. PIN Nos. IN BRACKETS REFER TO SUB-BOARDS PRIOR TO ISSUE 4.

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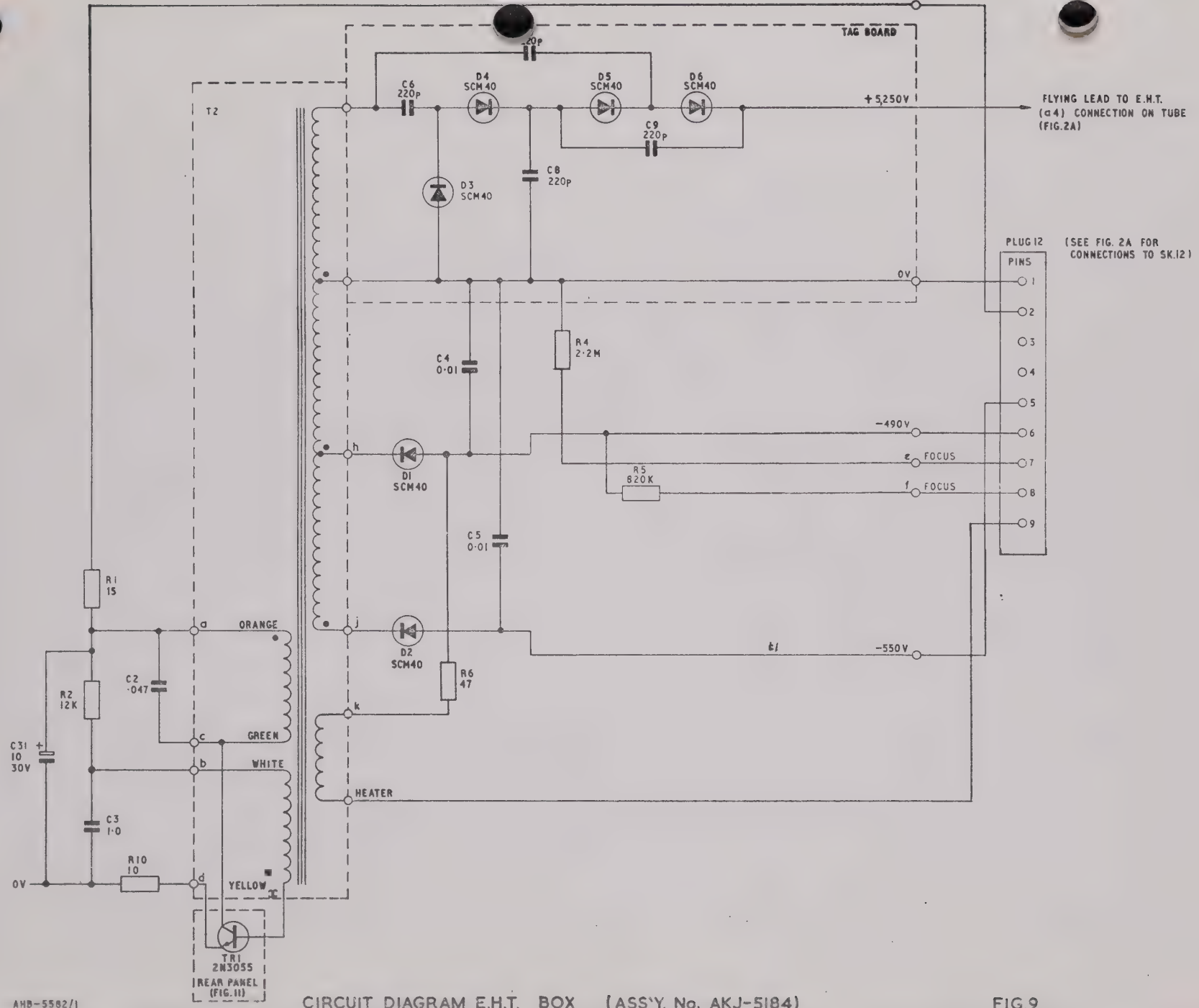
CIRCUIT DIAGRAM SUB-BOARD (ASSY. No. AKJ-5173)

FIG.8



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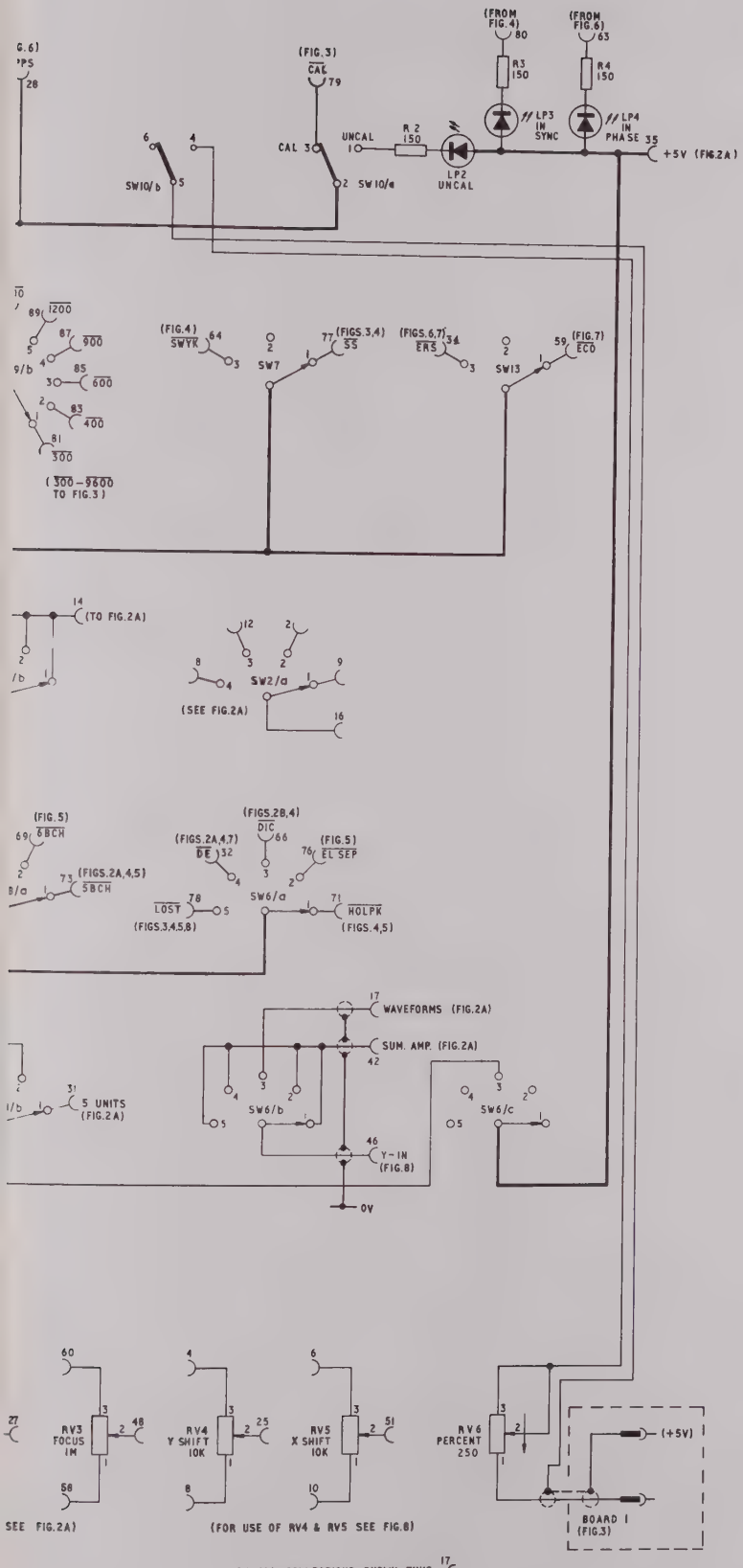
CIRCUIT DIAGRAM E.H.T. BOX (ASS'Y. No. AKJ-5184)

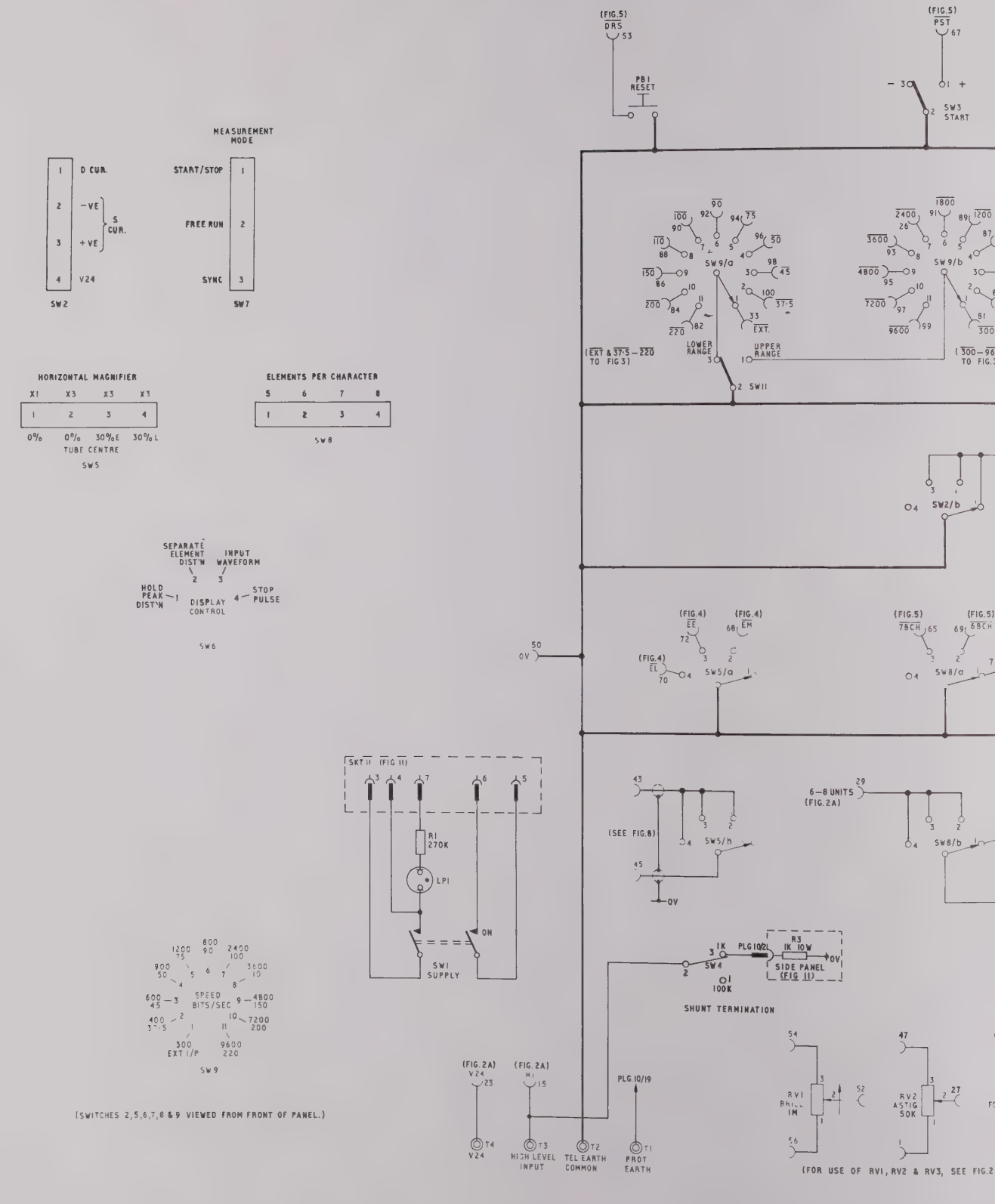
FIG.9

CIRCUIT DIAGRAM OF COMPONENTS ON FRONT PANEL TYPE 1A



NOTE :- ALL CONNECTIONS SHOWN THUS 17 ARE ON THE 100-WAY EDGE CONNECTION TO THE MOTHER BOARD.

FIG.10A



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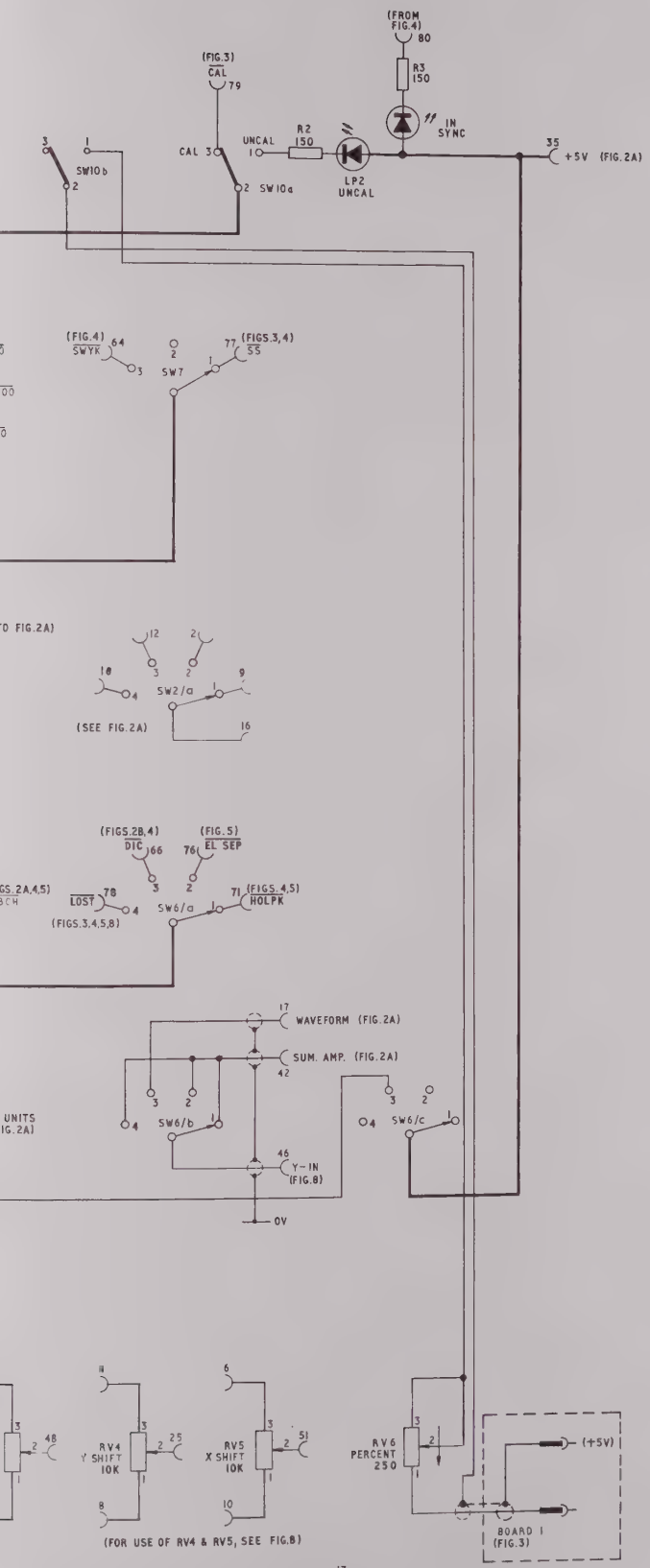
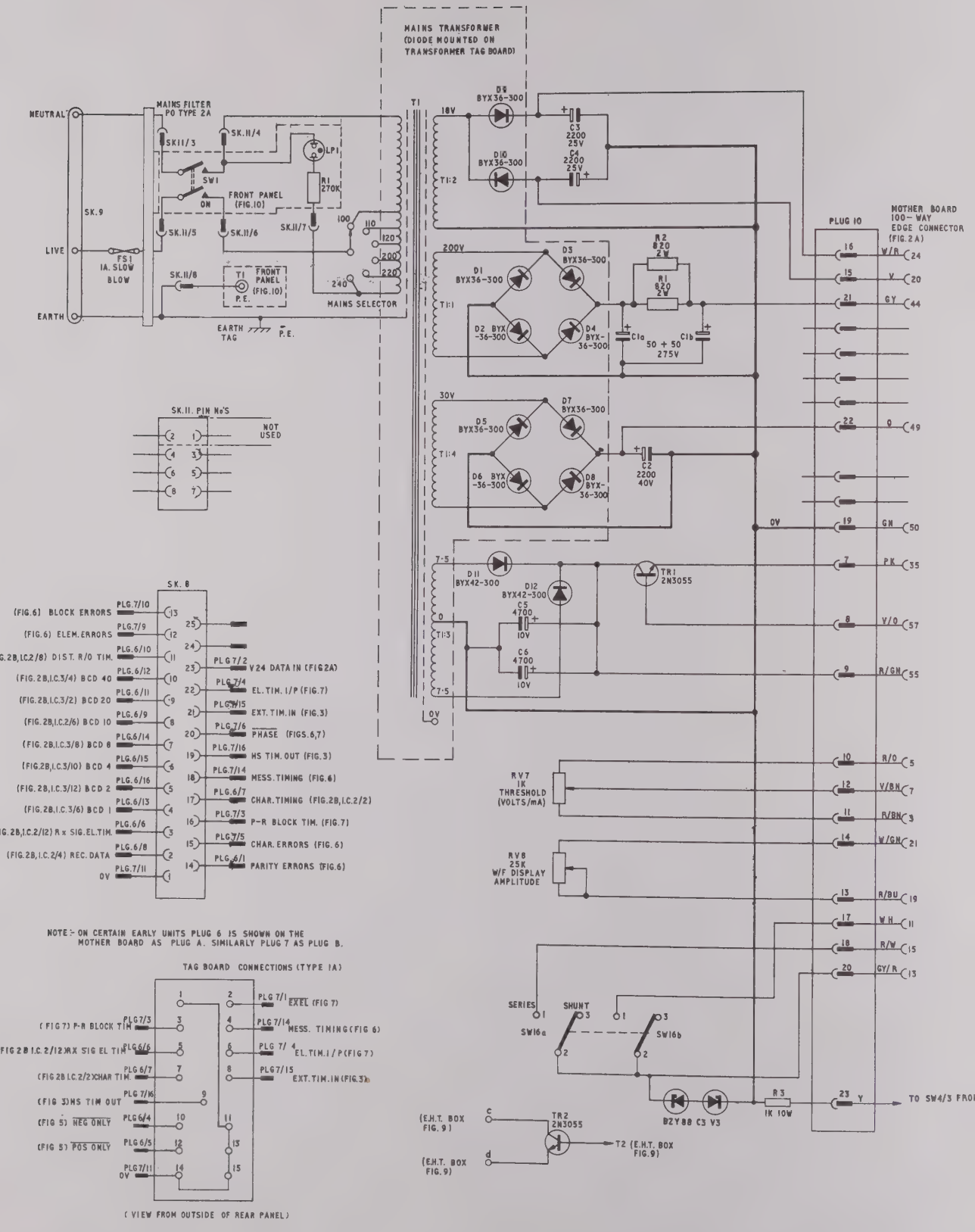
CIRCUIT DIAGRAM OF COMPONENTS ON FRONT PANEL TYPE 2A



NOTE:- ALL CONNECTIONS SHOWN THUS 17 ARE ON THE 100-WAY EDGE CONNECTION TO THE MOTHER BOARD.

FIG 10B



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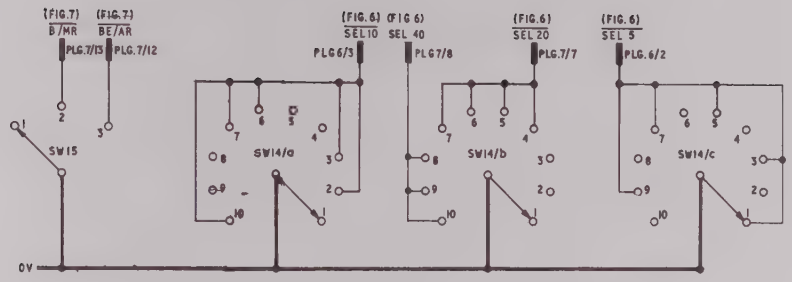
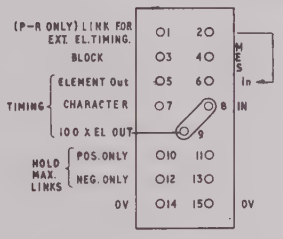
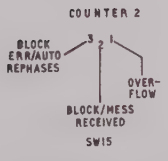
CIRCUIT DIAGRAM OF COMPONENTS O



(VIEWED FROM OUTSIDE OF REAR PANEL)

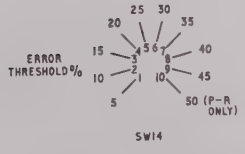
TAG BOARD ANNOTATION (TYPE 1A)





(VIEWED FROM OUTSIDE OF REAR PANEL)

(VIEWED FROM OUTSIDE OF REAR PANEL)

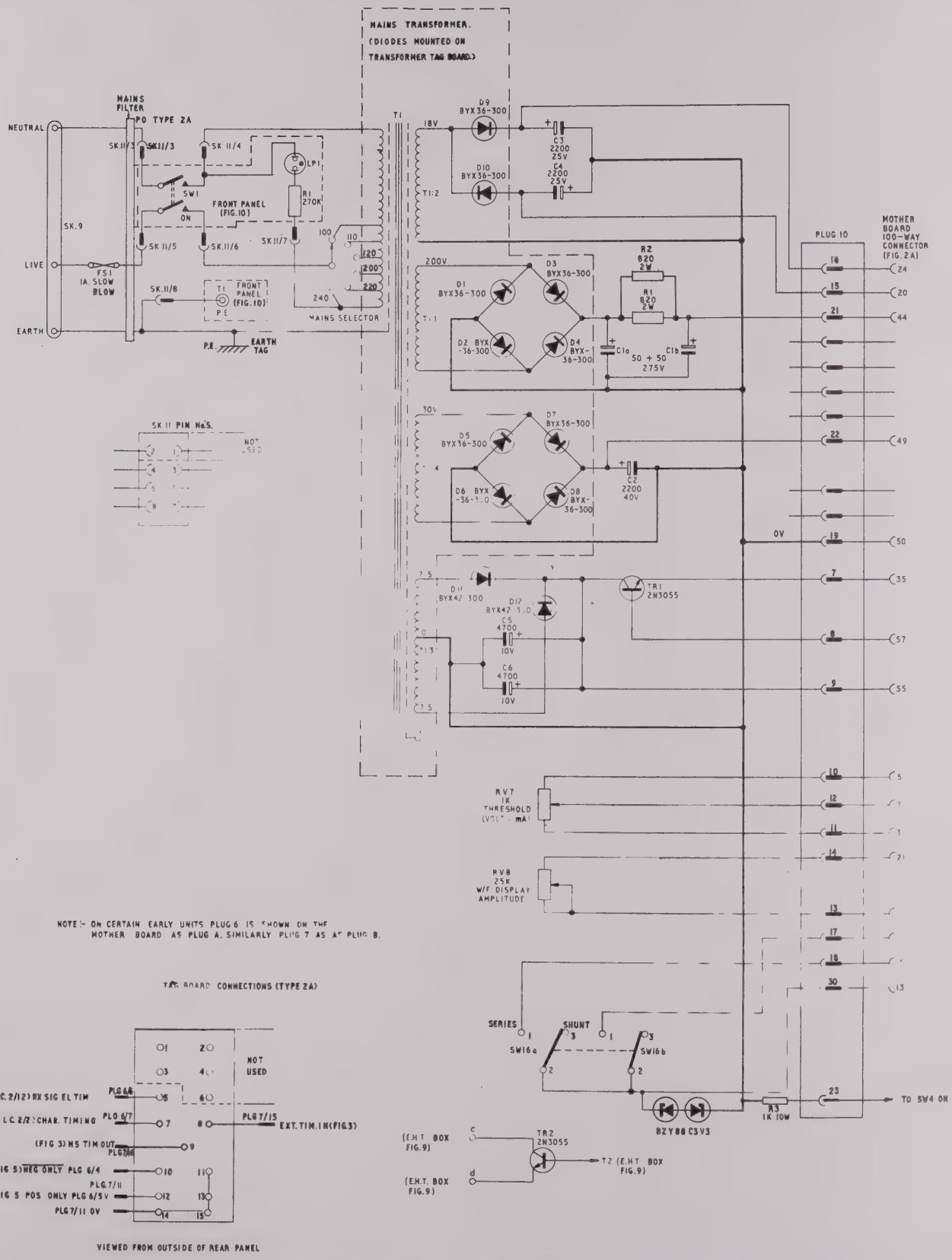


(VIEWED FROM OUTSIDE OF REAR PANEL)

PANEL (FIG 10)

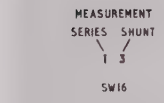
N REAR & SIDE PANELS. TYPE 1A

FIG. 11A



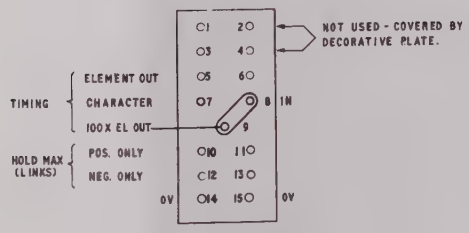
AHB7546

CIRCUIT DIAGRAM OF COMPONENTS ON REAR & SIDE PANELS. TYPE 2A



(VIEWED FROM OUTSIDE OF REAR PANEL)

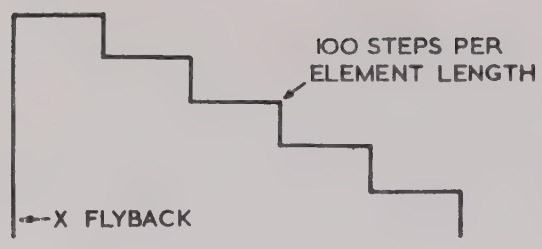
TAG BOARD ANNOTATION (TYPE 2A)



(VIEWED FROM OUTSIDE OF REAR PANEL)

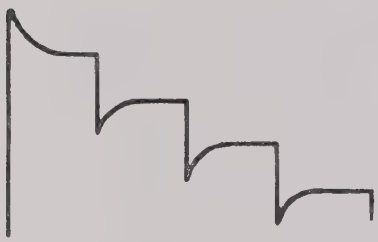
ONT PANEL (FIG 10)

FIG. 11B



IDEAL x SCAN WAVEFORM

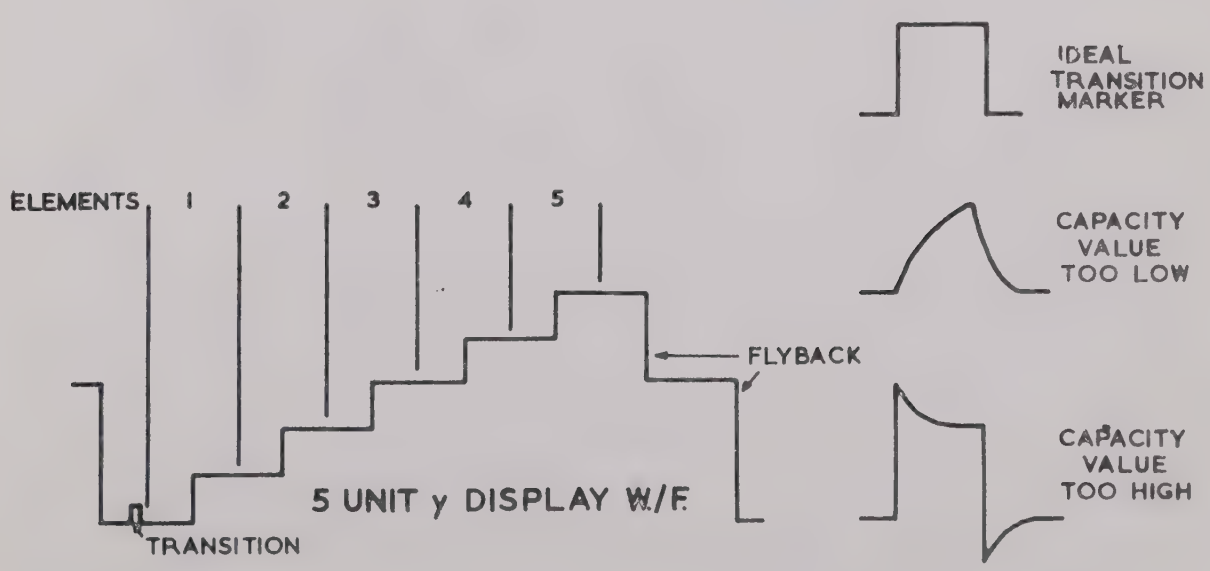
CAPACITY VALUE TOO LOW



CAPACITY VALUE TOO HIGH

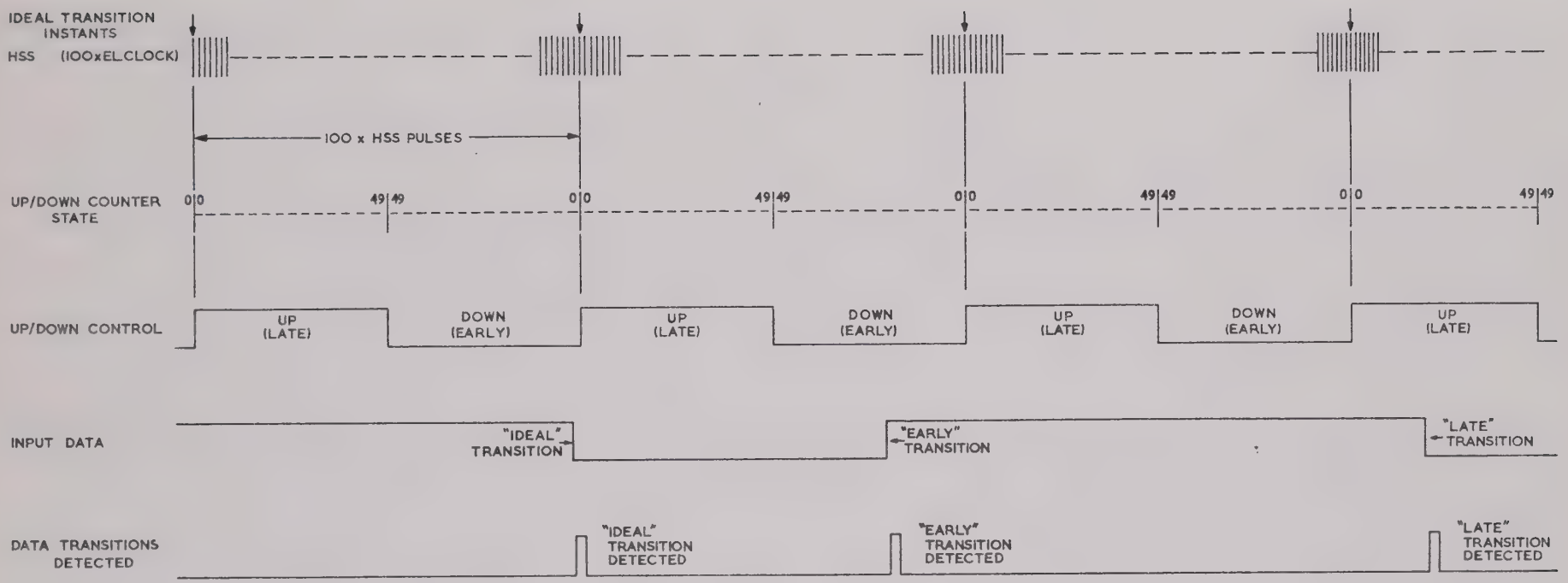
x SCAN AMPLIFIER H.F. COMPENSATION (4·3·4)

FIG. 12A



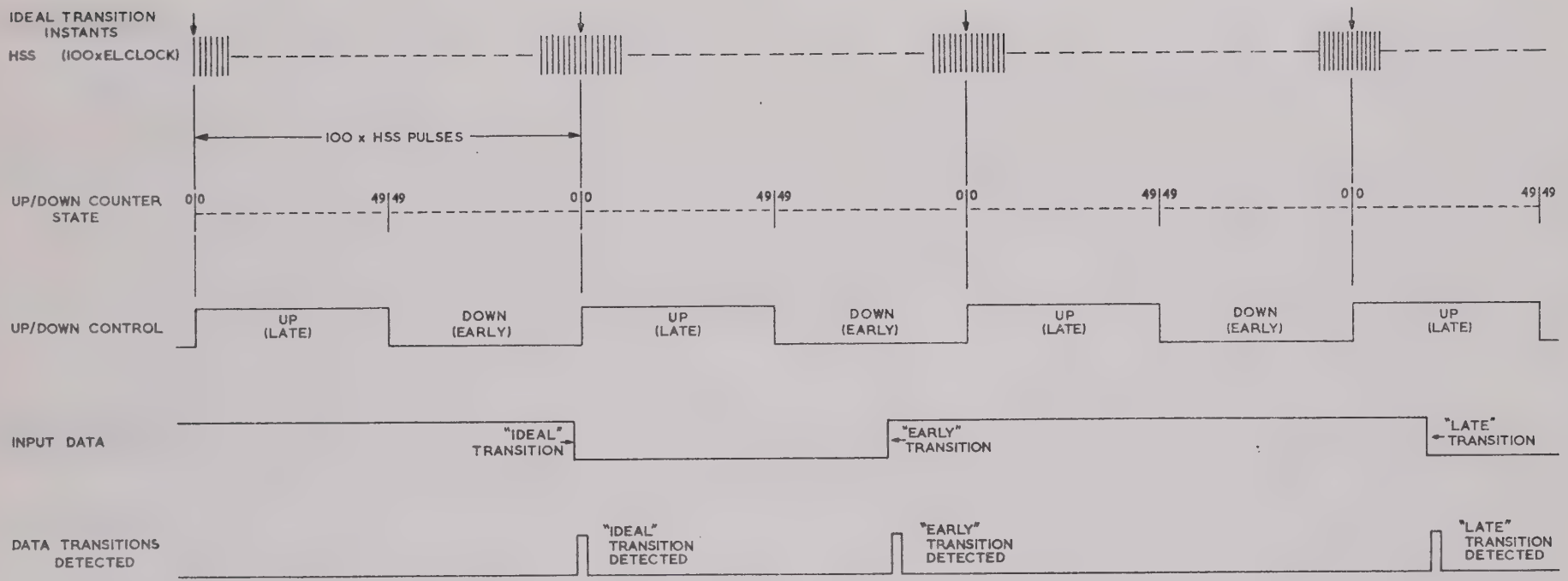
y SCAN AMPLIFIER H.F. COMPENSATION (4·3·7)

FIG. 12B



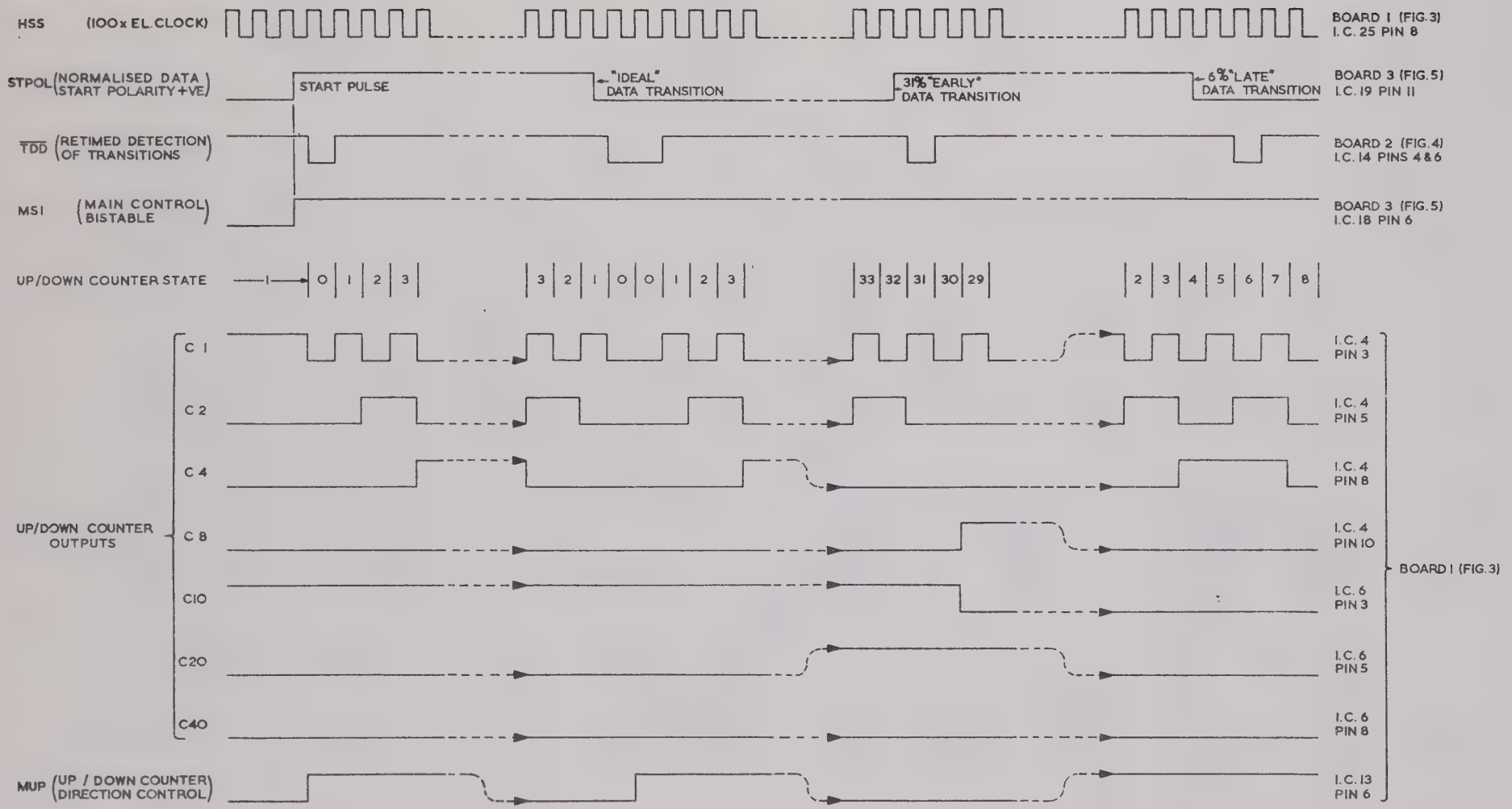
RELATIONSHIP OF UP/DOWN COUNTER TO INCOMING DATA TRANSITIONS

FIG. 12C



RELATIONSHIP OF UP/DOWN COUNTER TO INCOMING DATA TRANSITIONS

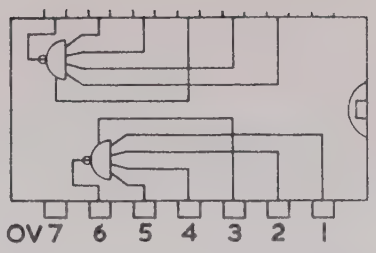
FIG. 12C


HSS (100x EL. CLOCK)
BOARD 1 (FIG.3) I.C. 25 PIN 8
STPOL (NORMALISED DATA START POLARITY +VE)
START PULSE
"IDEAL" DATA TRANSITION
31% "EARLY" DATA TRANSITION
6% "LATE" DATA TRANSITION
BOARD 3 (FIG.5) I.C. 19 PIN 11
TDD (RETIMED DETECTION OF TRANSITIONS)
BOARD 2 (FIG.4) I.C. 14 PINS 4 & 6
MSI (MAIN CONTROL BISTABLE)
BOARD 3 (FIG.5) I.C. 18 PIN 6
UP/DOWN COUNTER STATE
-1 0 1 2 3 3 2 1 0 0 1 2 3 33 32 31 30 29 2 3 4 5 6 7 8
UP/DOWN COUNTER OUTPUTS
C1
C2
C4
C8
C10
C20
C40
I.C. 4 PIN 3
I.C. 4 PIN 5
I.C. 4 PIN 8
I.C. 4 PIN 10
I.C. 6 PIN 3
I.C. 6 PIN 5
I.C. 6 PIN 8
BOARD 1 (FIG.3)
MUP (UP / DOWN COUNTER DIRECTION CONTROL)
I.C. 13 PIN 6

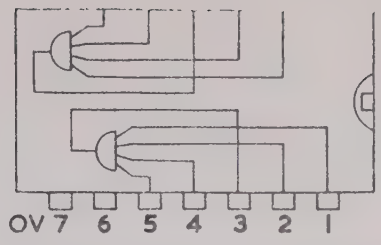
RELATIONSHIP OF UP/DOWN COUNTER TO START ELEMENT TRANSITION AND SUBSEQUENT TRANSITIONS DISTORTED BY VARIOUS AMOUNTS.

FIG. 12D

930 DUAL 4 INPUT NAND GATE

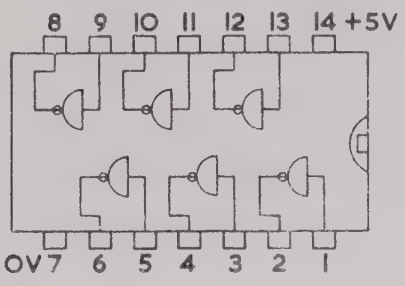


933 DUAL 4 INPUT EXPANDER



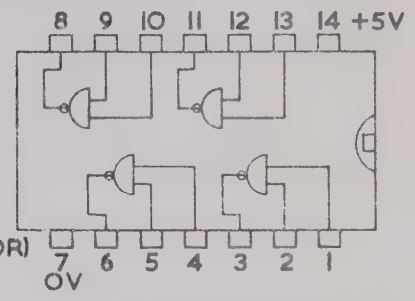
932 DUAL INPUT BUFFER

936 HEX INVERTER

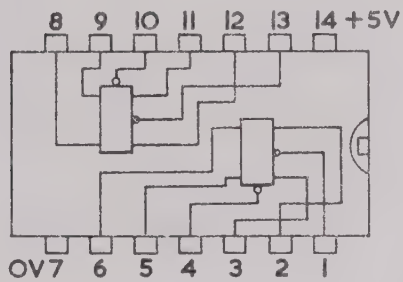


946 QUAD 2 INPUT NAND GATE

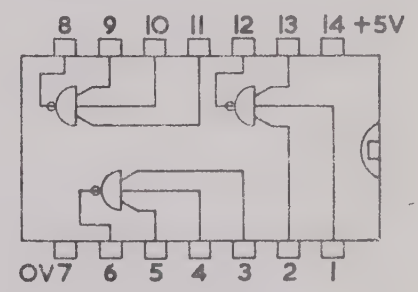
DM 8810 QUAD HIGH LEVEL DRIVER (OPEN COLLECTOR)



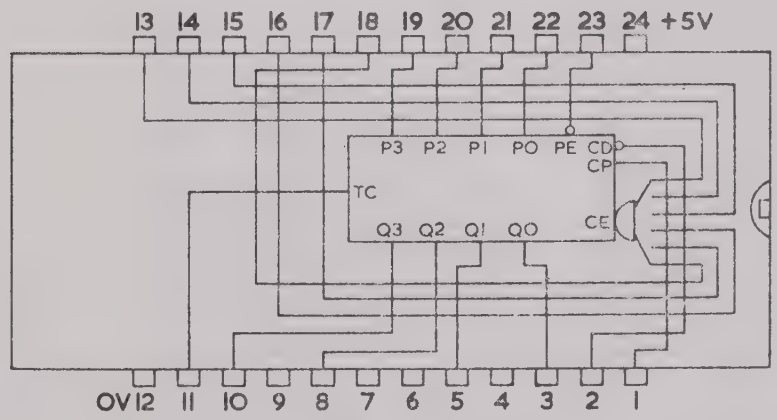
9093 DUAL CLOCKED JK FLIP-FLOPS



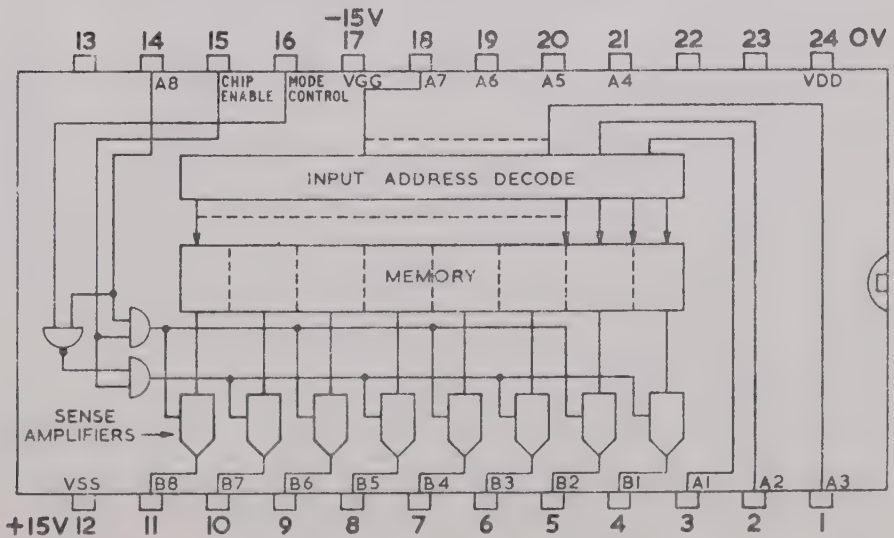
962 TRIPLE 3 INPUT NAND GATE



9306 10-WAY UP/DOWN BCD COUNTER



MM5220 1024-BIT READ ONLY MEMORY


−15V
13 14 15 16 17 18 19 20 21 22 23 24 OV
A8
CHIP ENABLE
MODE CONTROL
VGG
A7 A6 A5 A4
VDD
INPUT ADDRESS DECODE
MEMORY
SENSE AMPLIFIERS
VSS
B8 B7 B6 B5 B4 B3 B2 B1 A1 A2 A3
+15V 12 11 10 9 8 7 6 5 4 3 2 1

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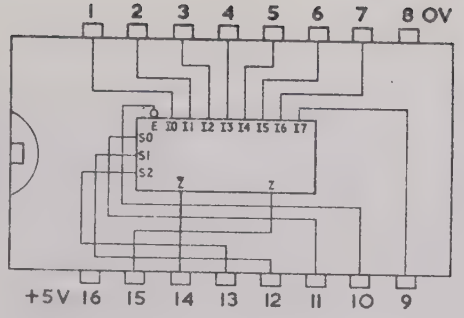
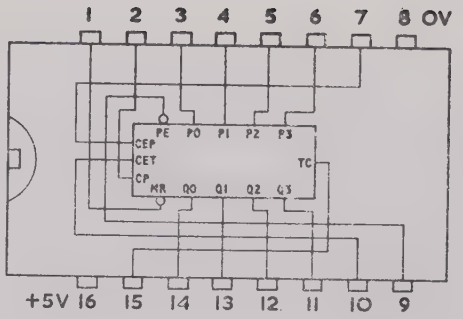
I.C. CONNECTIONS

FIG.13 A

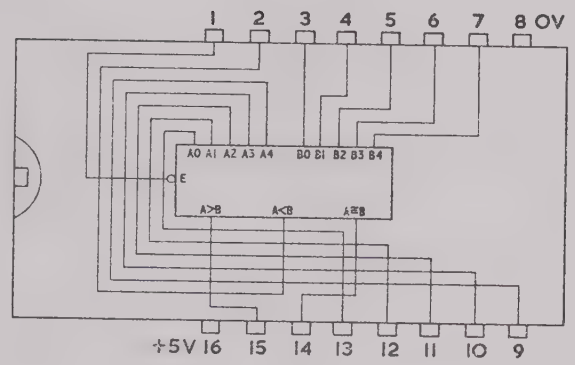
9312. 8 INPUT MULTIPLEXER.



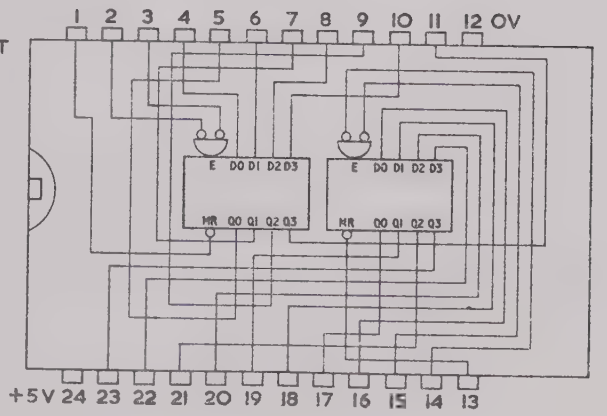
9310 BCD DECADE COUNTER.



9324. 5 BIT COMPARATOR.



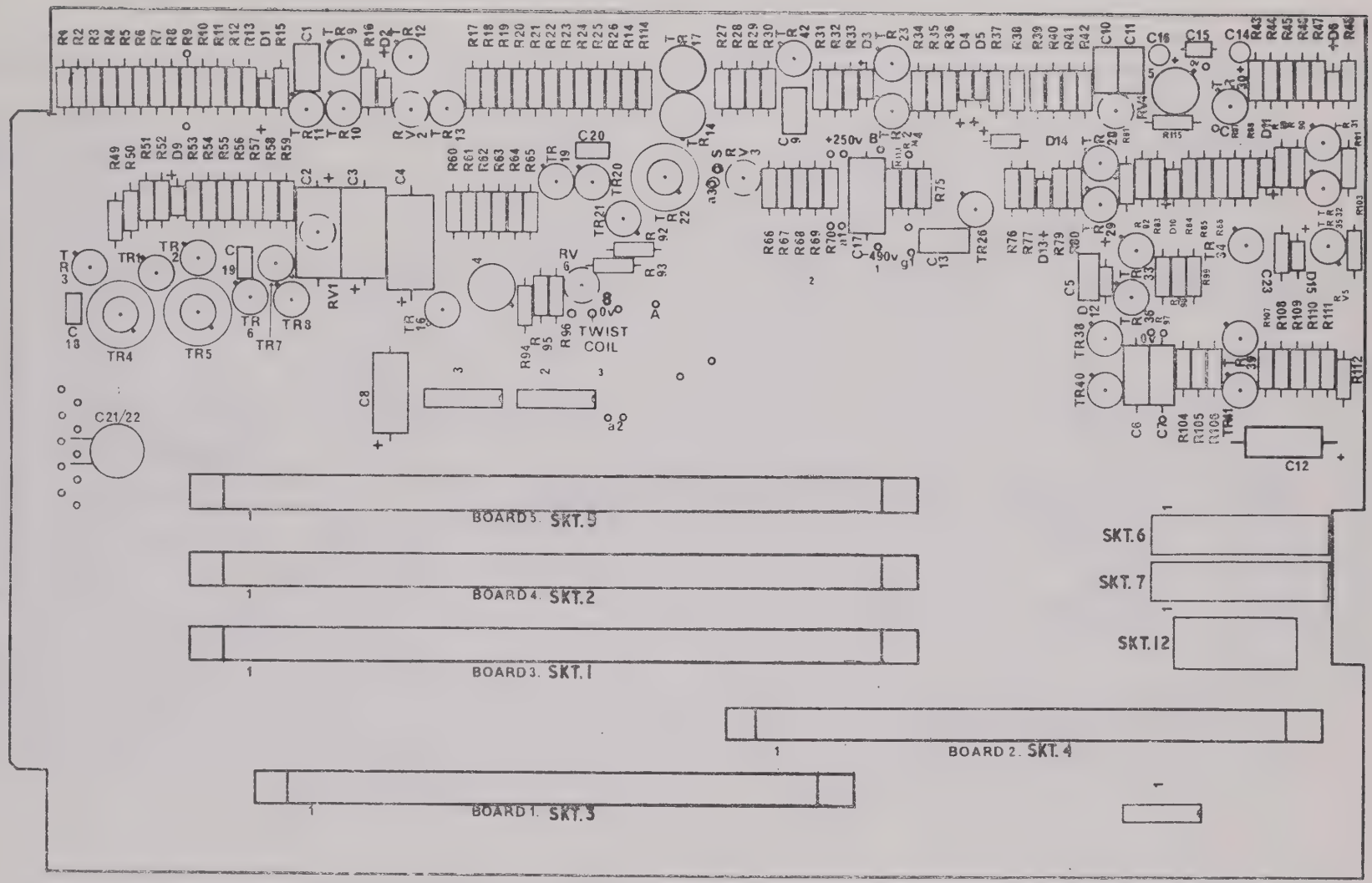
9308 DUAL 4 BIT LATCH.



AMB-5584 B/1

I.C. CONNECTIONS.

FIG.13 B



NOTE:- OMIT BOARDS 4&5 FOR TYPE II

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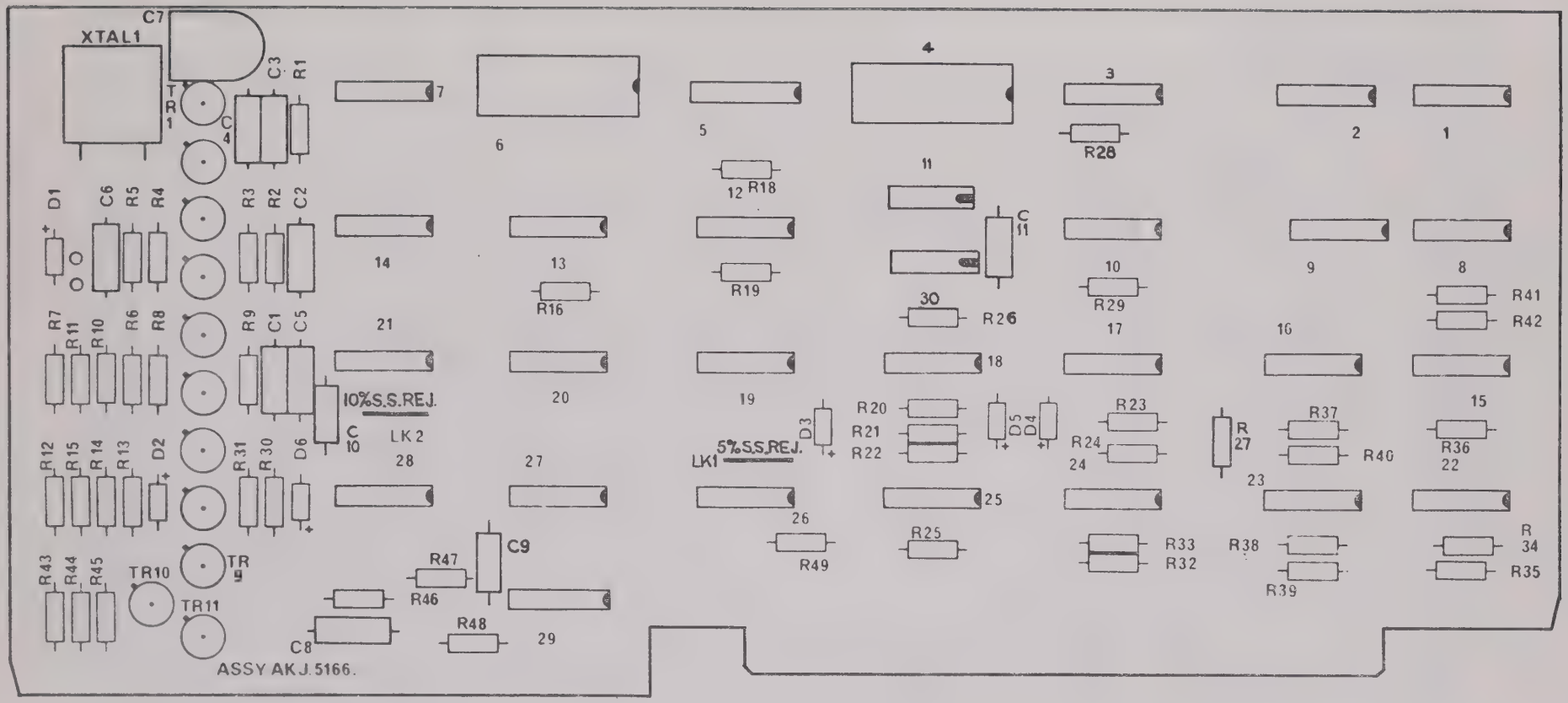
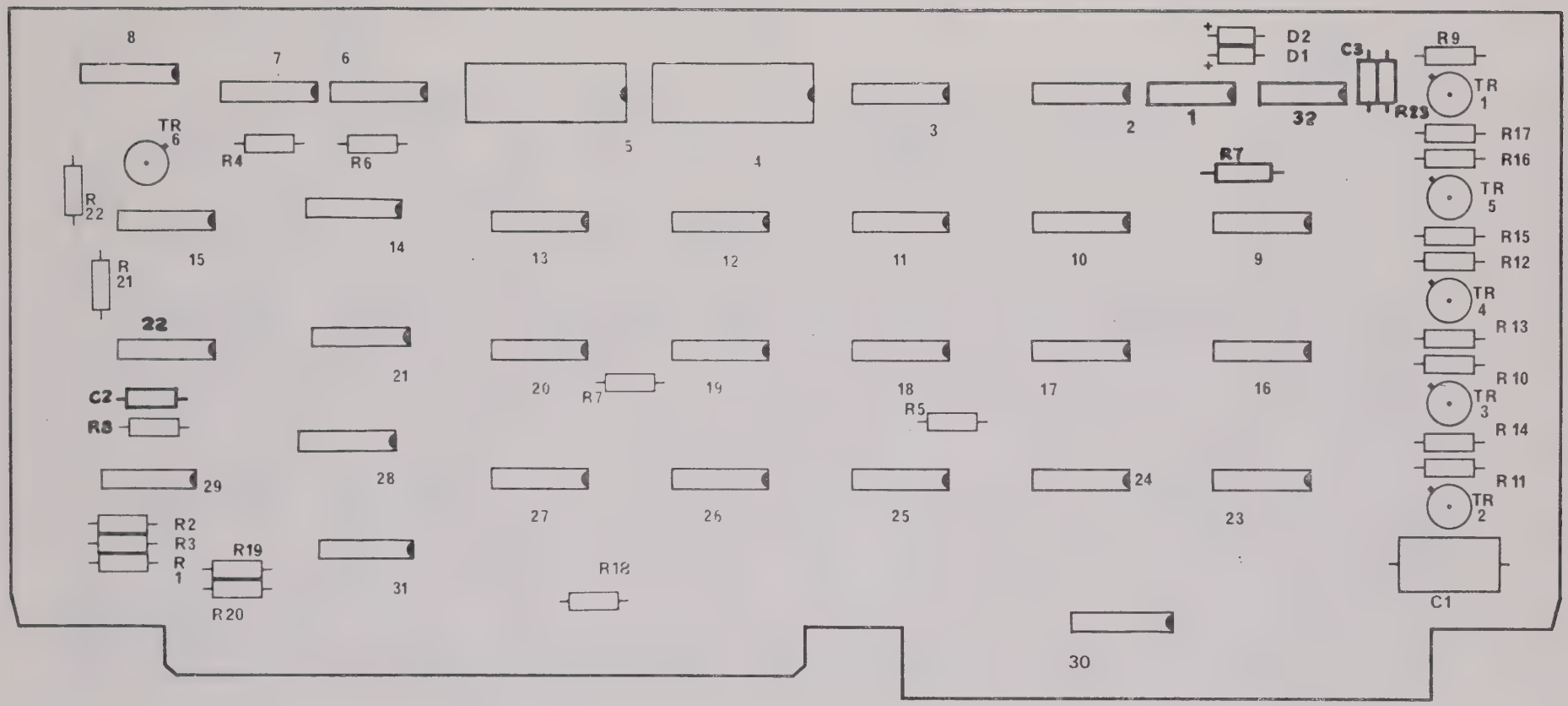
MOTHER BOARD ASSEMBLY

FIG. 14



AHB-5586/1 LOGIC BOARD 1 ASSEMBLY FIG.15



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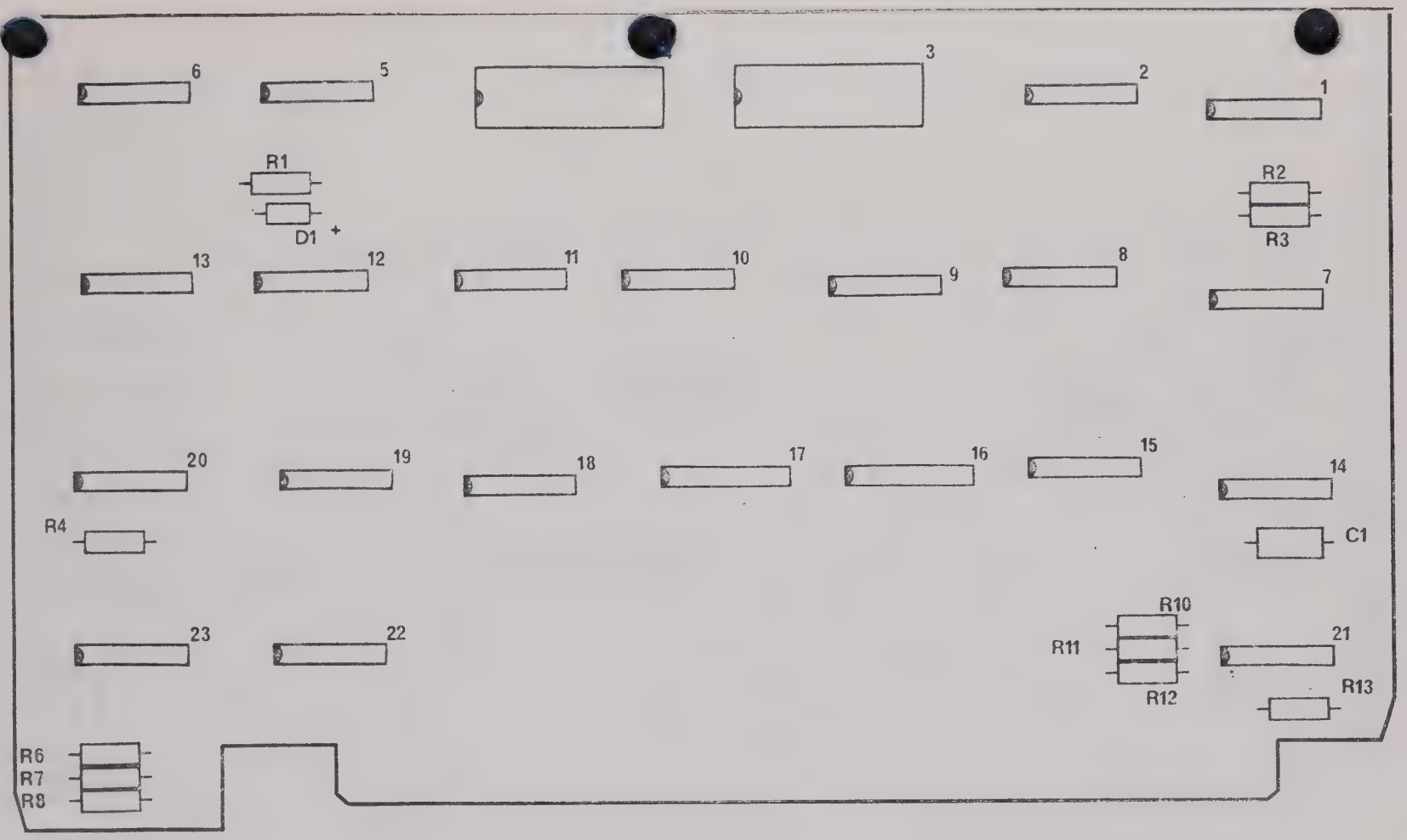
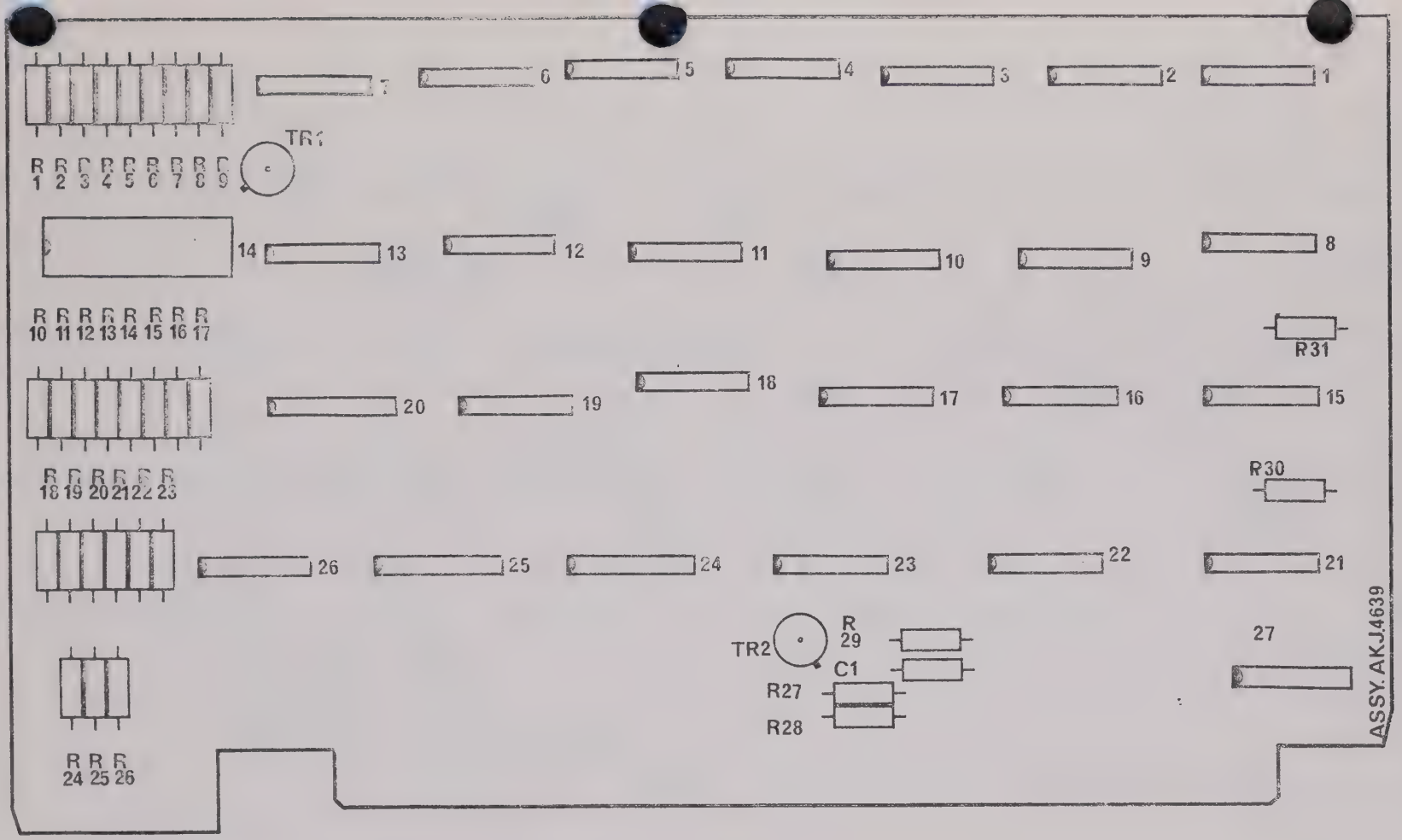
LOGIC BOARD 2 ASSEMBLY

FIG. 16



AHB-5588/1 LOGIC BOARD 3 ASSEMBLY FIG.17



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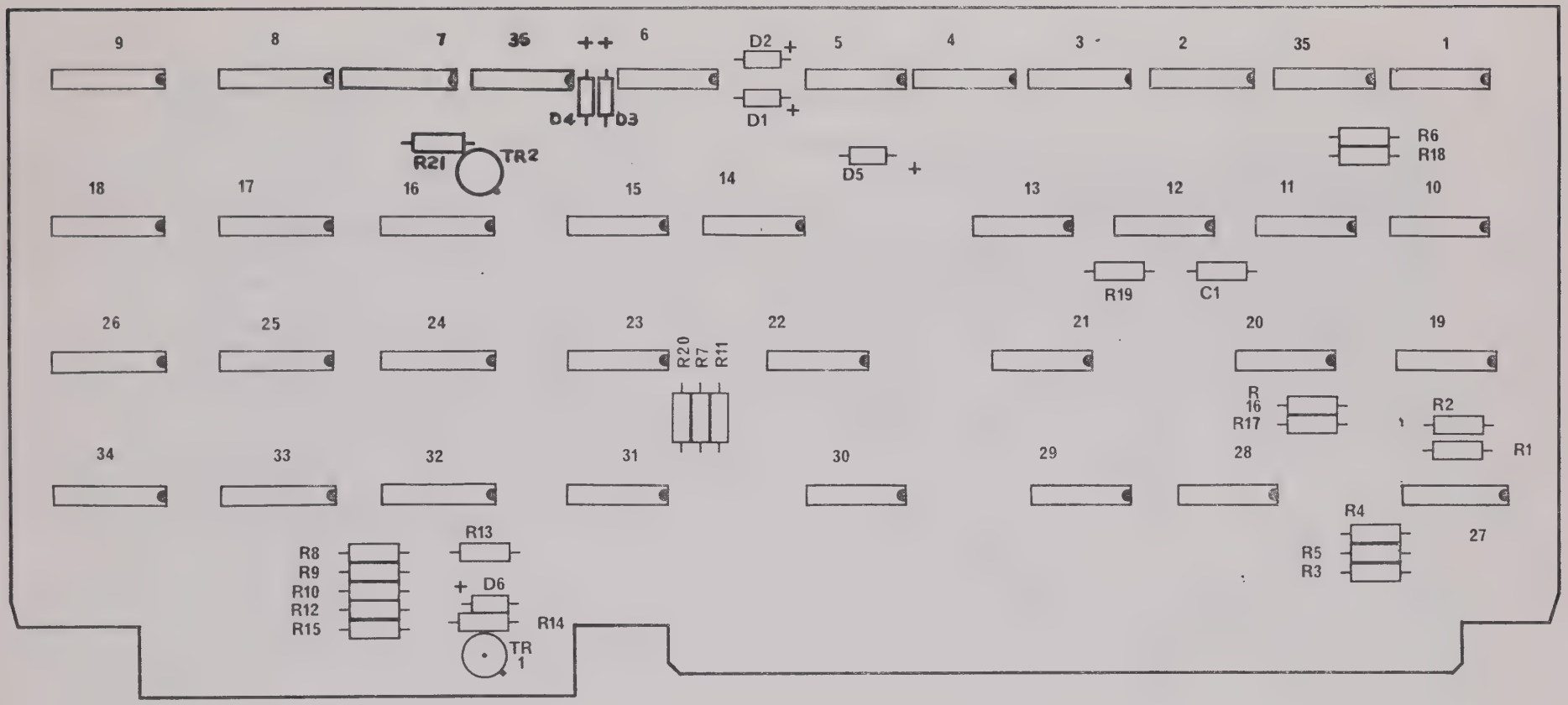
LOGIC BOARD 4 ASSEMBLY

FIG.18



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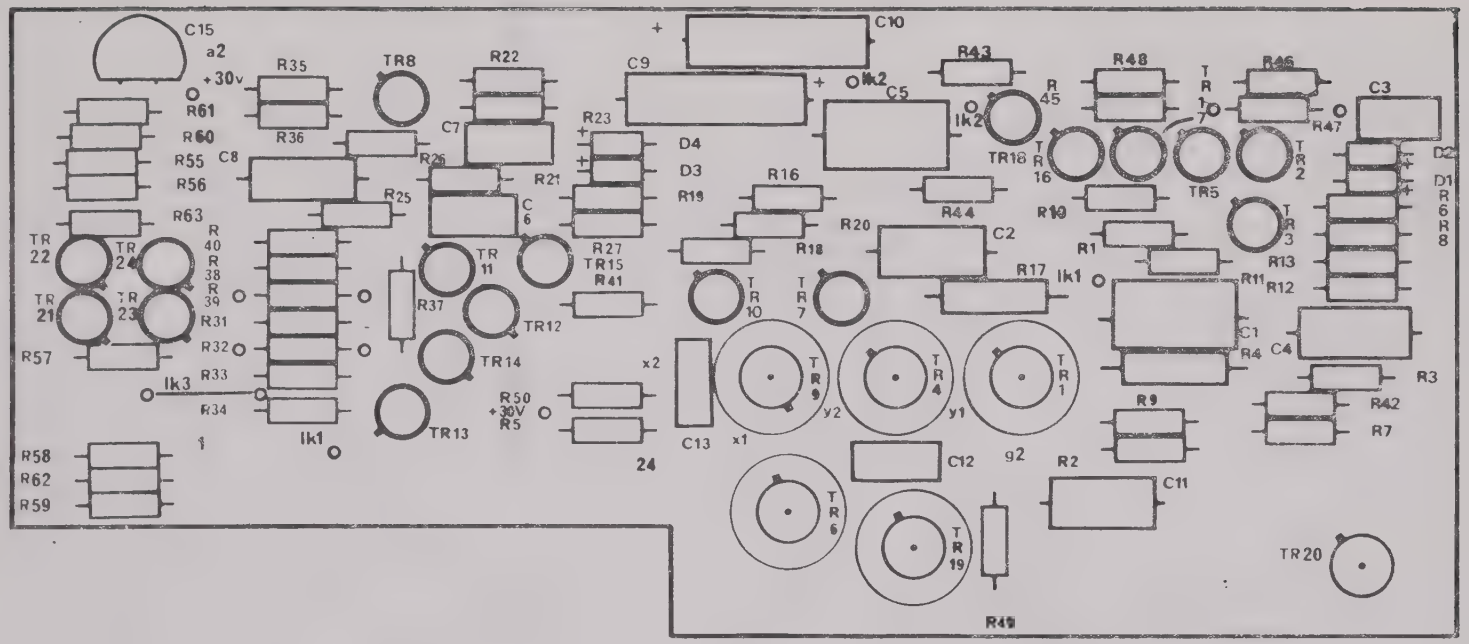
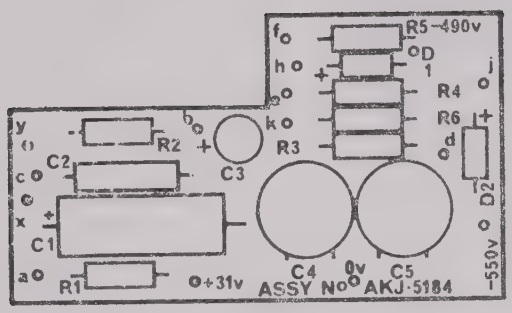
LOGIC BOARD 5 ASSEMBLY

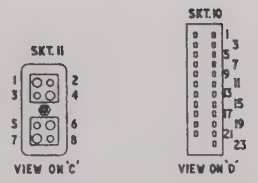
FIG. 19



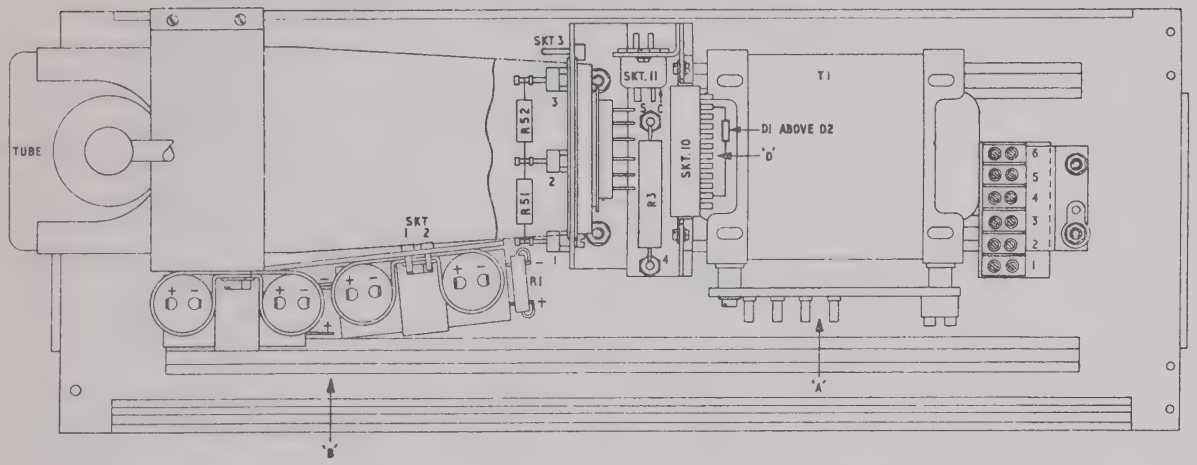
AHB-5591/1 SUB-BOARD ASSEMBLY FIG. 20



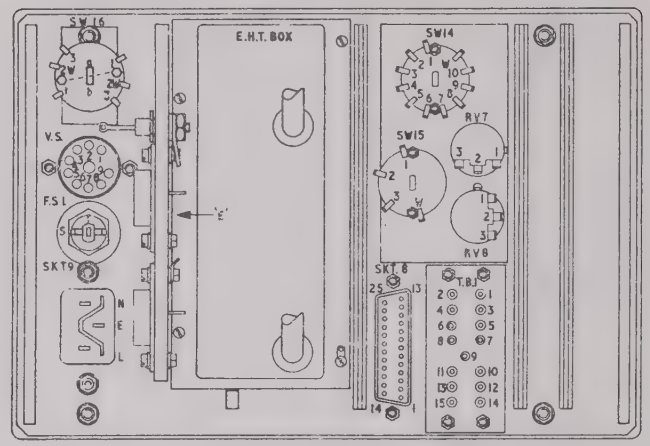
AHB-5593/1 E.H.T. BOARD ASSEMBLY FIG.21

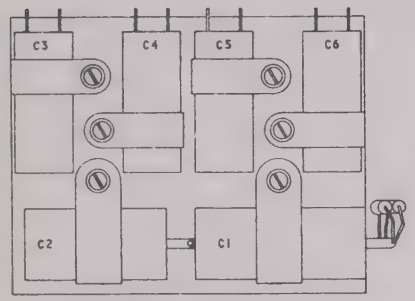


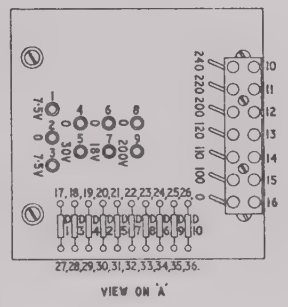
L.H. SIDE PANEL VIEWED FROM INSIDE UNIT. TYPES 1A & 2A



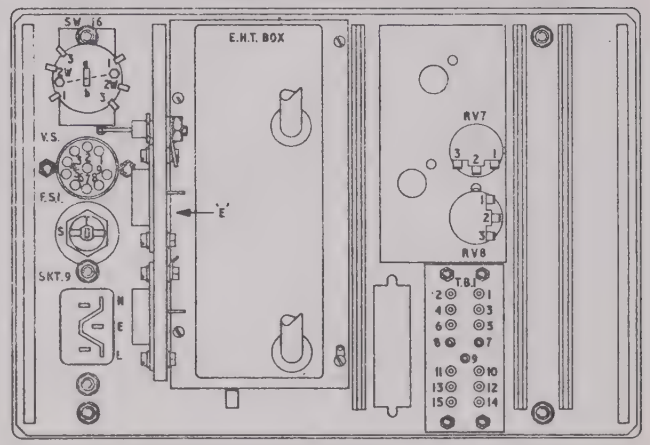
REAR PANEL VIEWED FROM INSIDE UNIT. TYPE 1A







REAR PANEL VIEWED FROM INSIDE UNIT. TYPE 2A



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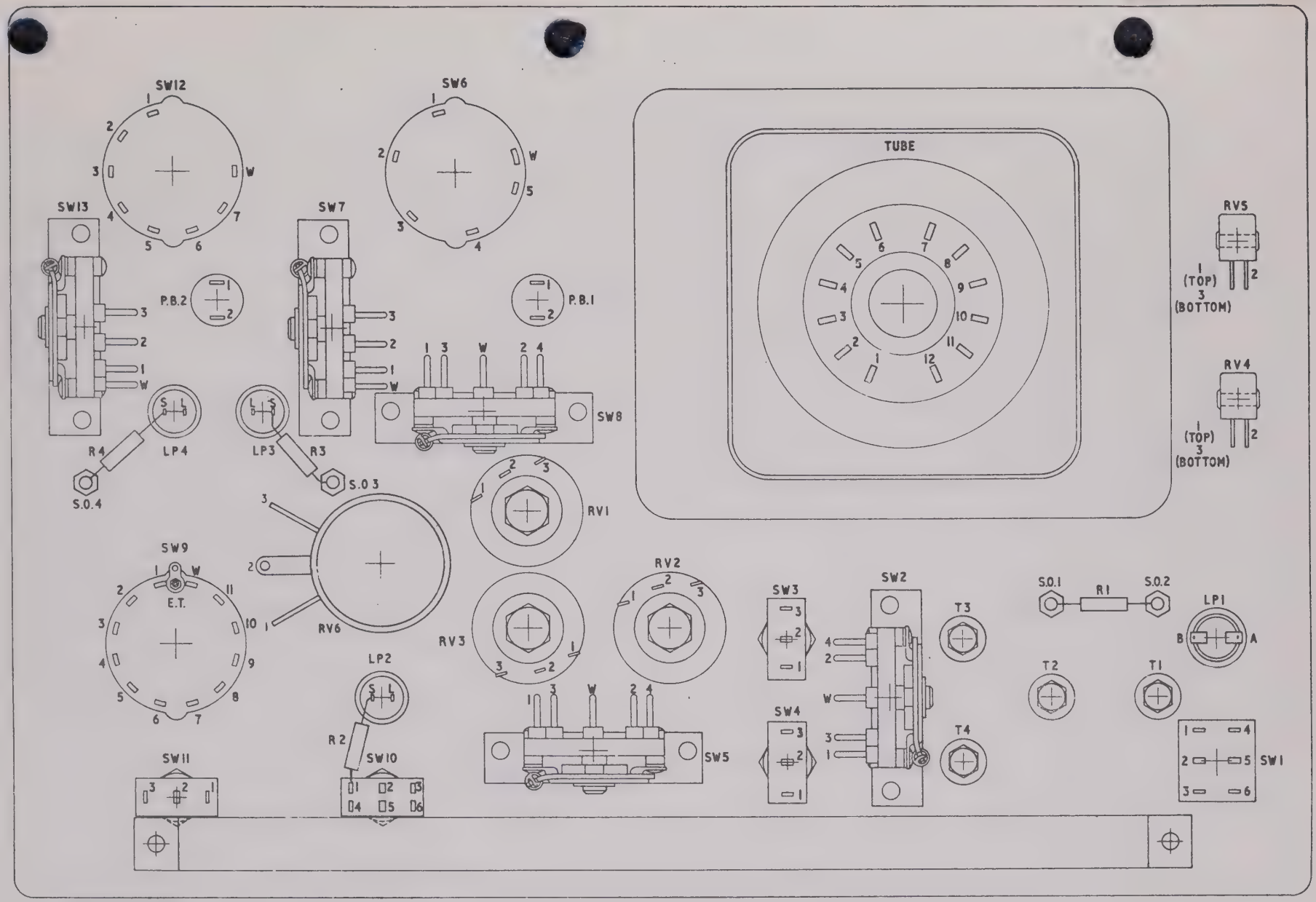
REAR & SIDE PANEL COMPONENT ASS'Y. TYPES 1A & 2A

FIG. 22



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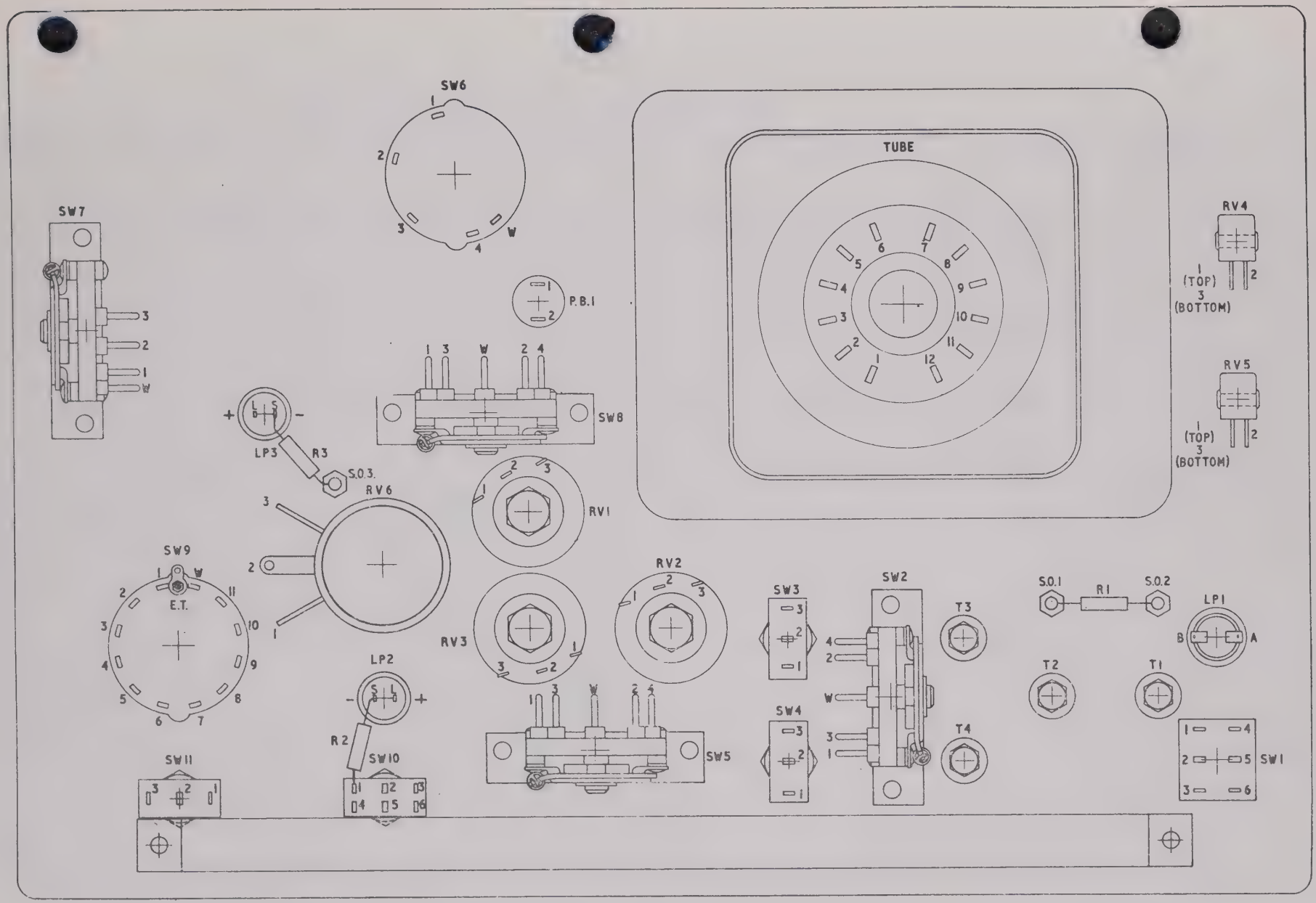
REAR VIEW. FRONT PANEL. TYPE 1A

FIG. 23A



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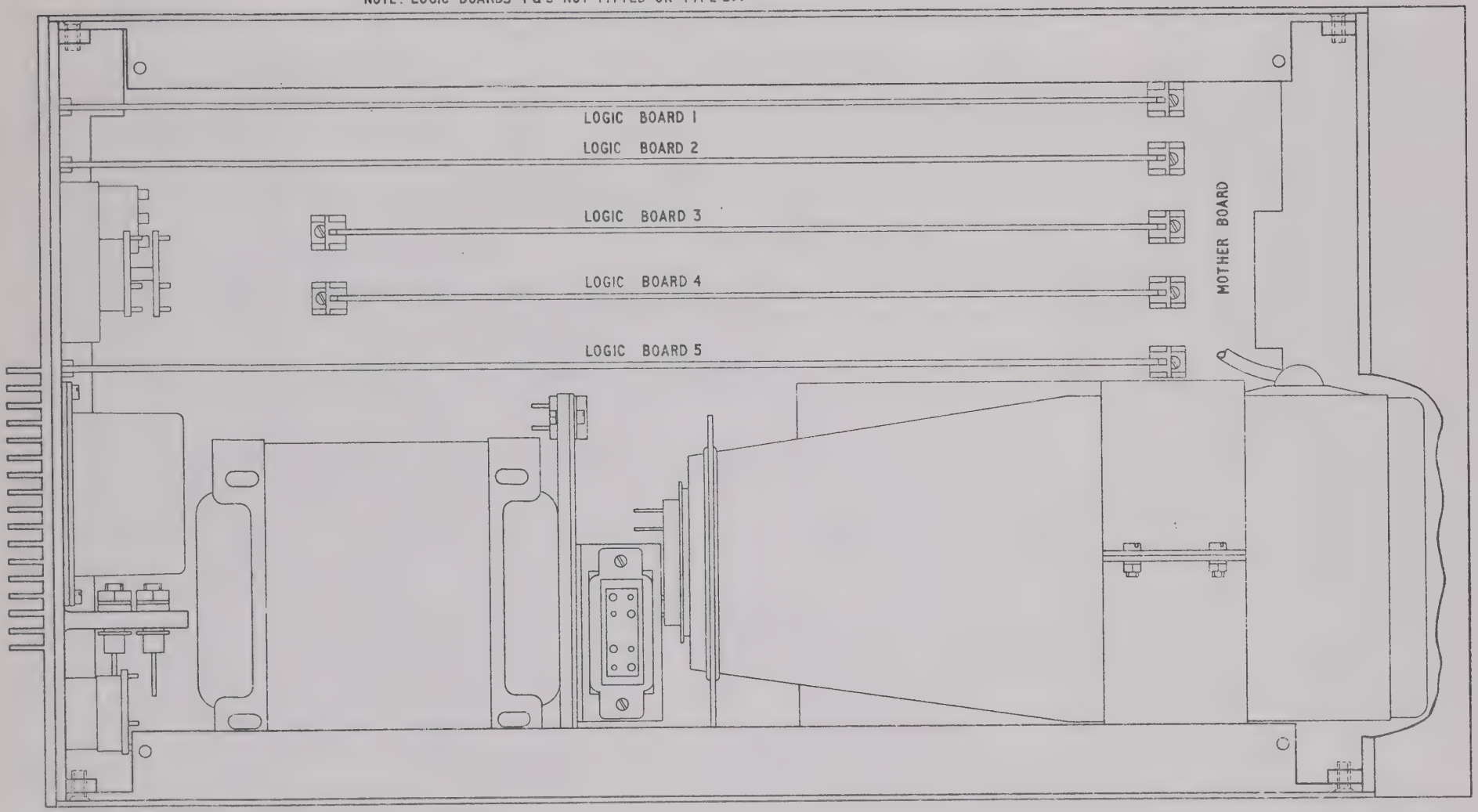
REAR VIEW. FRONT PANEL. TYPE 2A

FIG. 23B

VIEW FROM TOP WITH LID REMOVED.

NOTE:- LOGIC BOARDS 4 & 5 NOT FITTED ON TYPE 2A



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GENERAL ASS'Y.

FIG.24

AMENDMENT LIST. MODEL :- T.D.S.A. MK II

ITEM No.	HANDBOOK DESIGNATION	COMPONENT OR PART No.	DESCRIPTION OF CHANGE	DATE OF CHANGE	'TREND' CHANGE NOTE No.
1	FIG 3		C12 ADDED IN PARALLEL WITH C1.		
			C13 ADDED IN PARALLEL WITH C5.	22/5/73	2322
	5/2	LOGIC BOARD 1.	C12 & C13 ADDED. 0·1μf ERIE 811T. 30v.		
2	FIG 21	C10	ADD TO VIEW	4-6-73	2327
3	FIG 9	C10.	ADD. -ve END TO 0V, +ve TO PIN d	"	"
		R10	CHANGE TO R3	"	"
		C31	CHANGE TO C1	"	"
4	Sect. 5.8.2.	C3	VOLTAGE NOW 35v	"	"
		C10	ADD 1μf 35v STC TAG	"	"
5	Sect. 5.1	R44 TO R48, R77, R79, R80			
		R82 TO R85, R87 TO R90	CHANGE TO 2%	11-6-73	2329
		C21	CHANGE TO WIMA TROPYFOL F 630V 0·02μF	"	"
		C22	REMOVE	"	"
6	FIG 2A	C21	CHANGE TO 0·02μf	"	"
		C23	REMOVE	"	"
7					
8	FLT 2.2.3	SUBSECTION C	DELETE SUB SECTION C	5-7-73	2335
9	Sect 5.1	TR33	CHANGE TO BSX 29	13-7-73	2341
10	FIG 2A	"	" "	"	"
11	FIG 2A	C13.	CHANGE TO 0·01μF 630v	19-7-73	2346
		R30 & R40	" " 10K	"	"
		R64	" " 6K8	"	"
		R75	" " 3K3	"	"
12	FIG 3	R58	" " 3K3	"	"
13	Sect 5.1	C13. R30. 40. 64. 75	CHANGE AS ITEM 11	"	"
14	Sect 5.7	R58	" " " 12	"	"
15	FIG. 21	EHT BOARD ASSY AHB 5593/1	DRG. OF ASSY. AKJ 5184 DELETED	31-1-74	2384
	"	" AHB 5593/2	" " " AKJ 7930 ADDED	"	"
16	5.9.1	SW14	CHANGE FROM AKJ-7440-C TO AKB-7438-C	12-6-74	2438

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